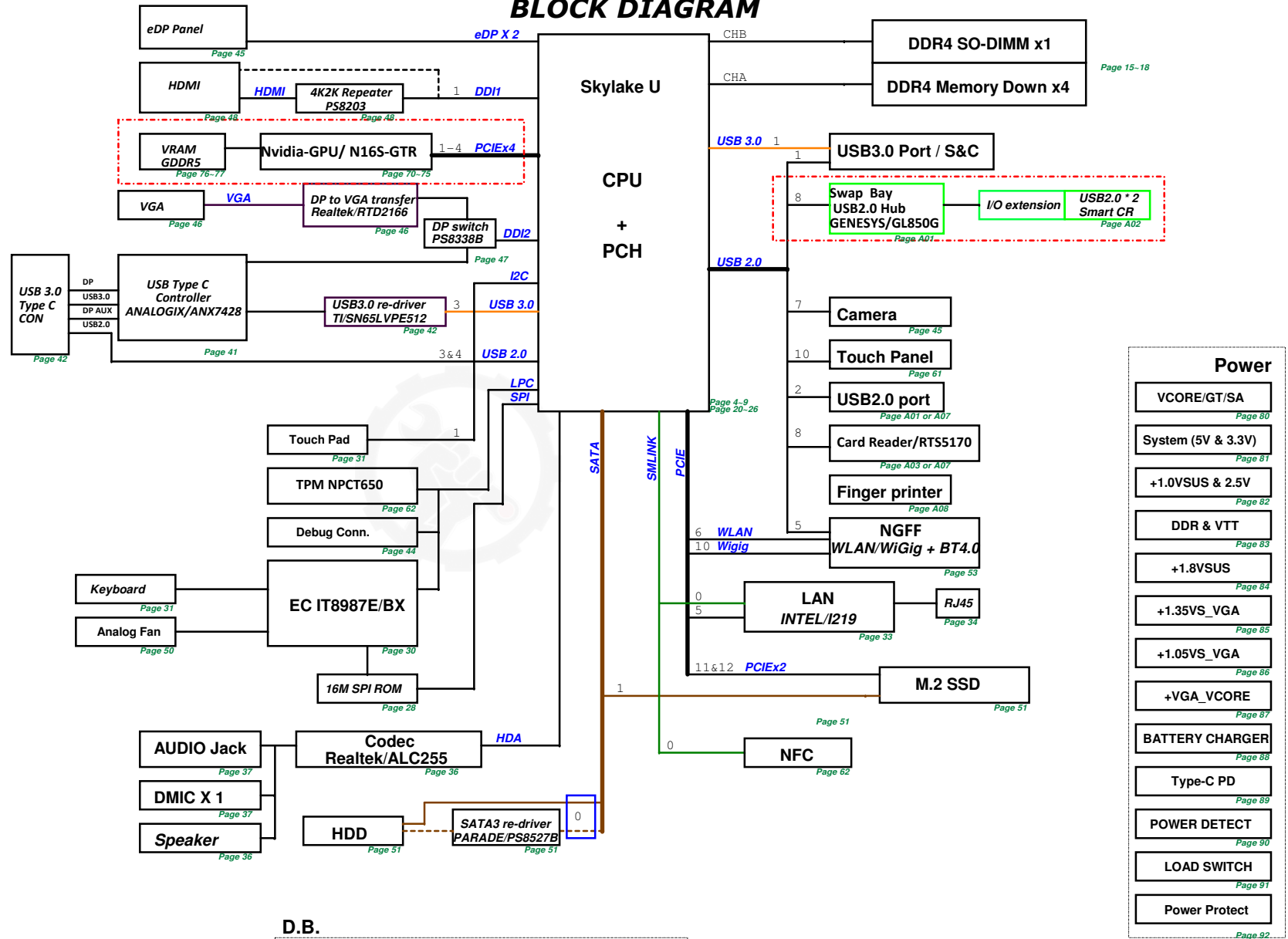
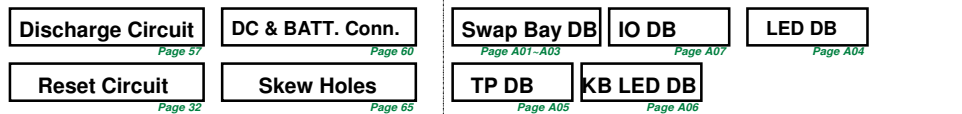


BLOCK DIAGRAM



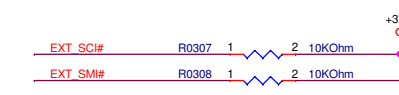
D.B.



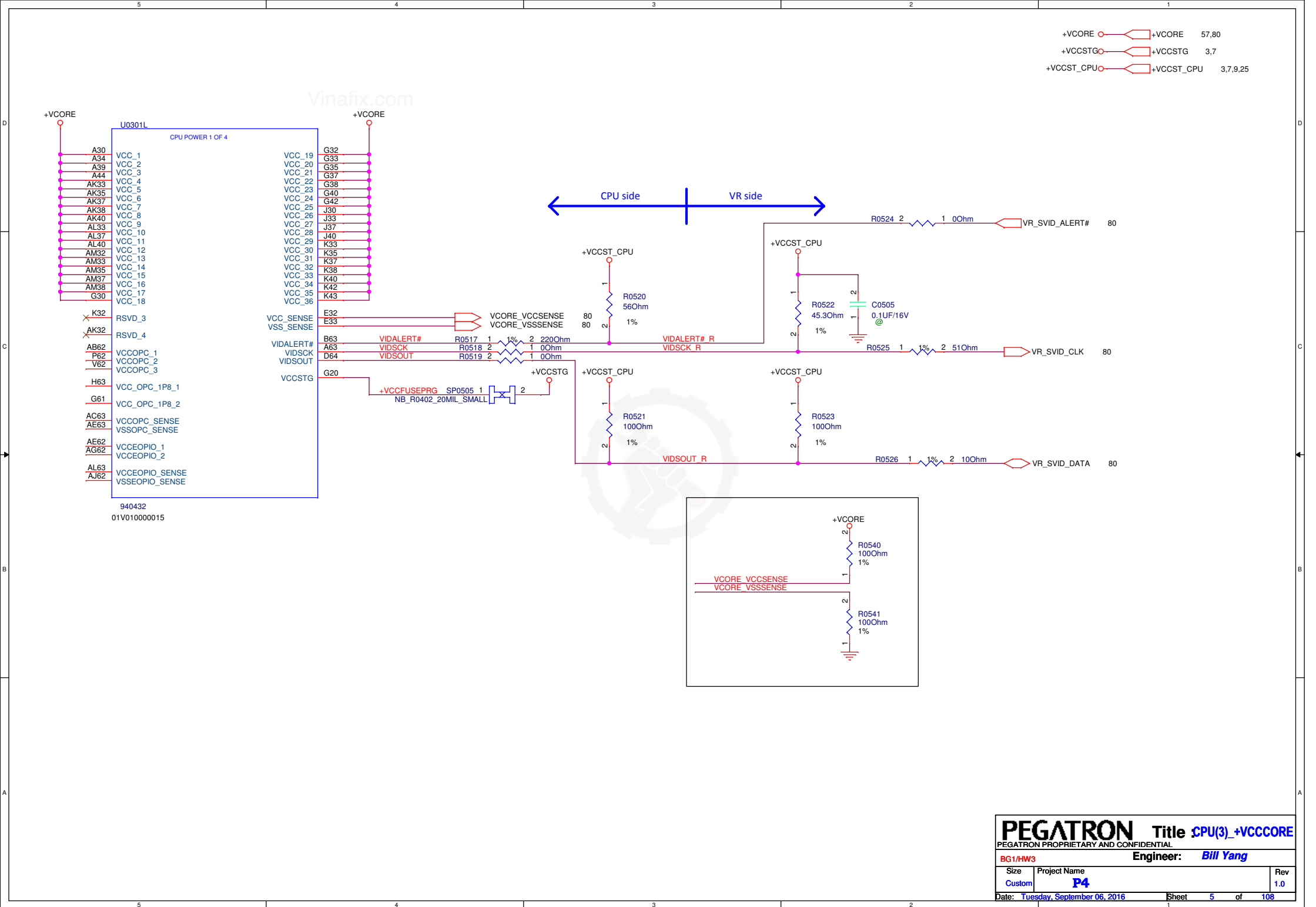
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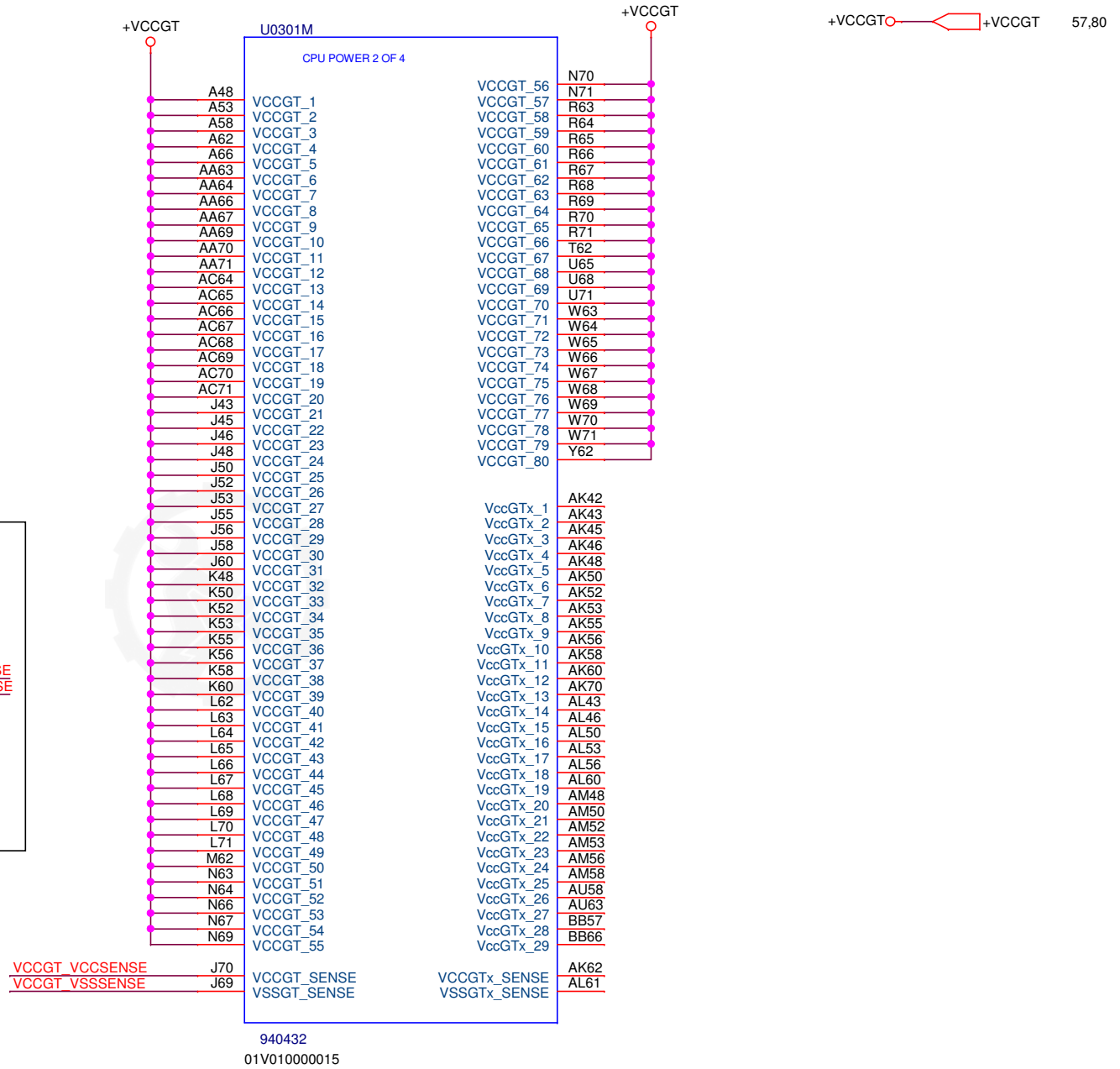
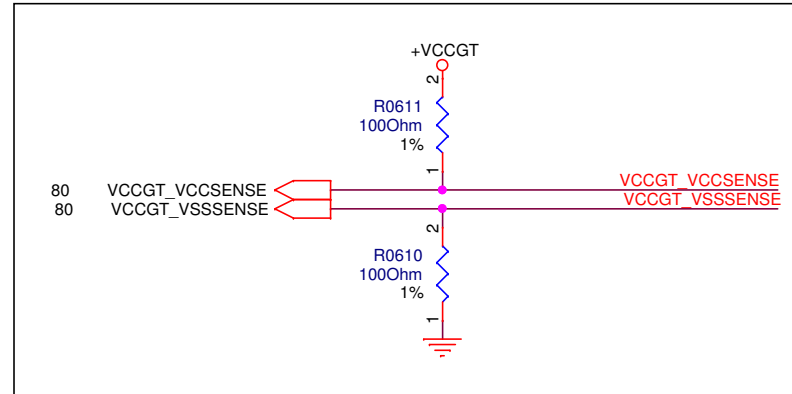
<Variant Name>			
PEGATRON Title :			
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Engineer:			
Size	Project Name	Date	Rev. 1
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Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect

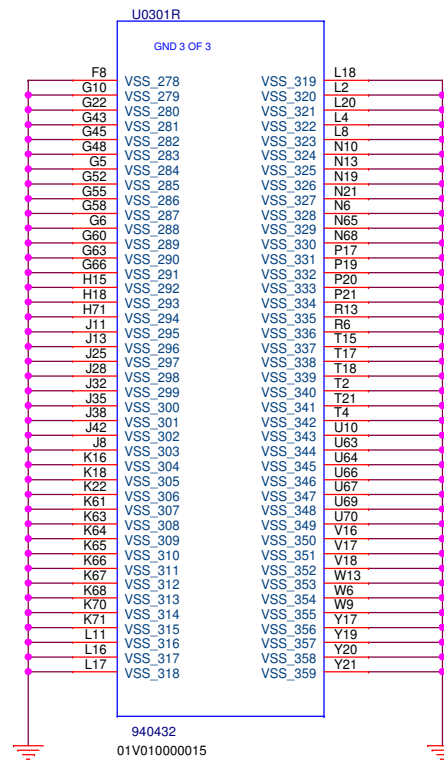
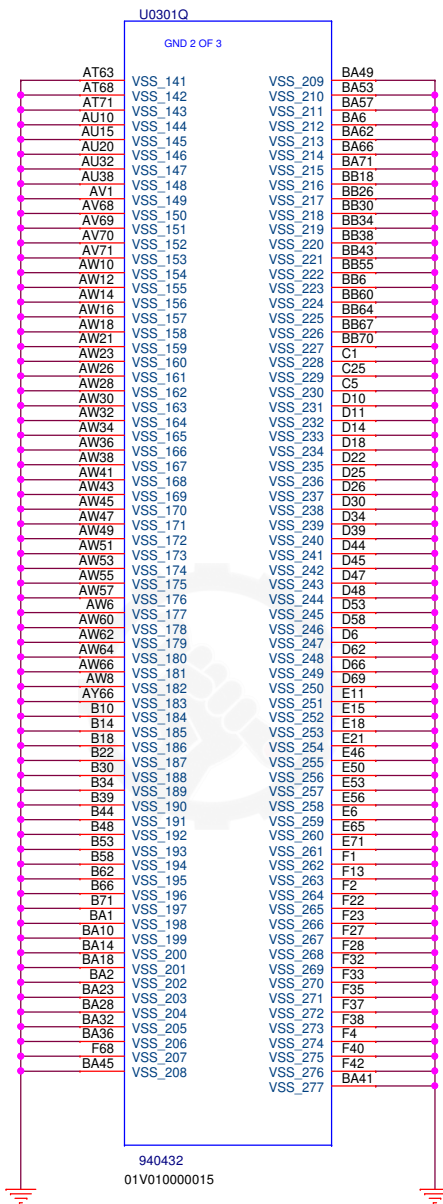
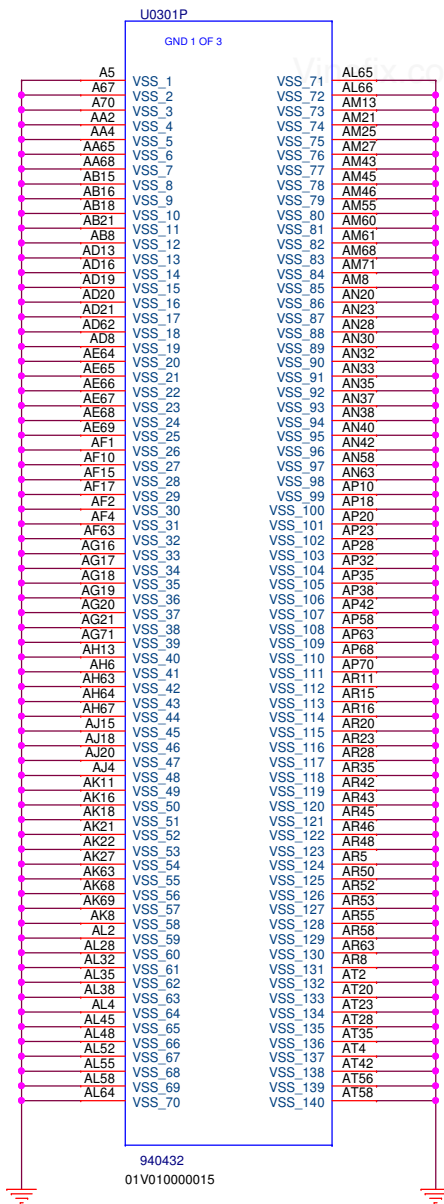


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PEGATRON		Title : CPU(4)_+VCCGT	
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BG1/HW3		Engineer: Bill Yang	
Size	Project Name	Rev	
Custom	P4	1.0	
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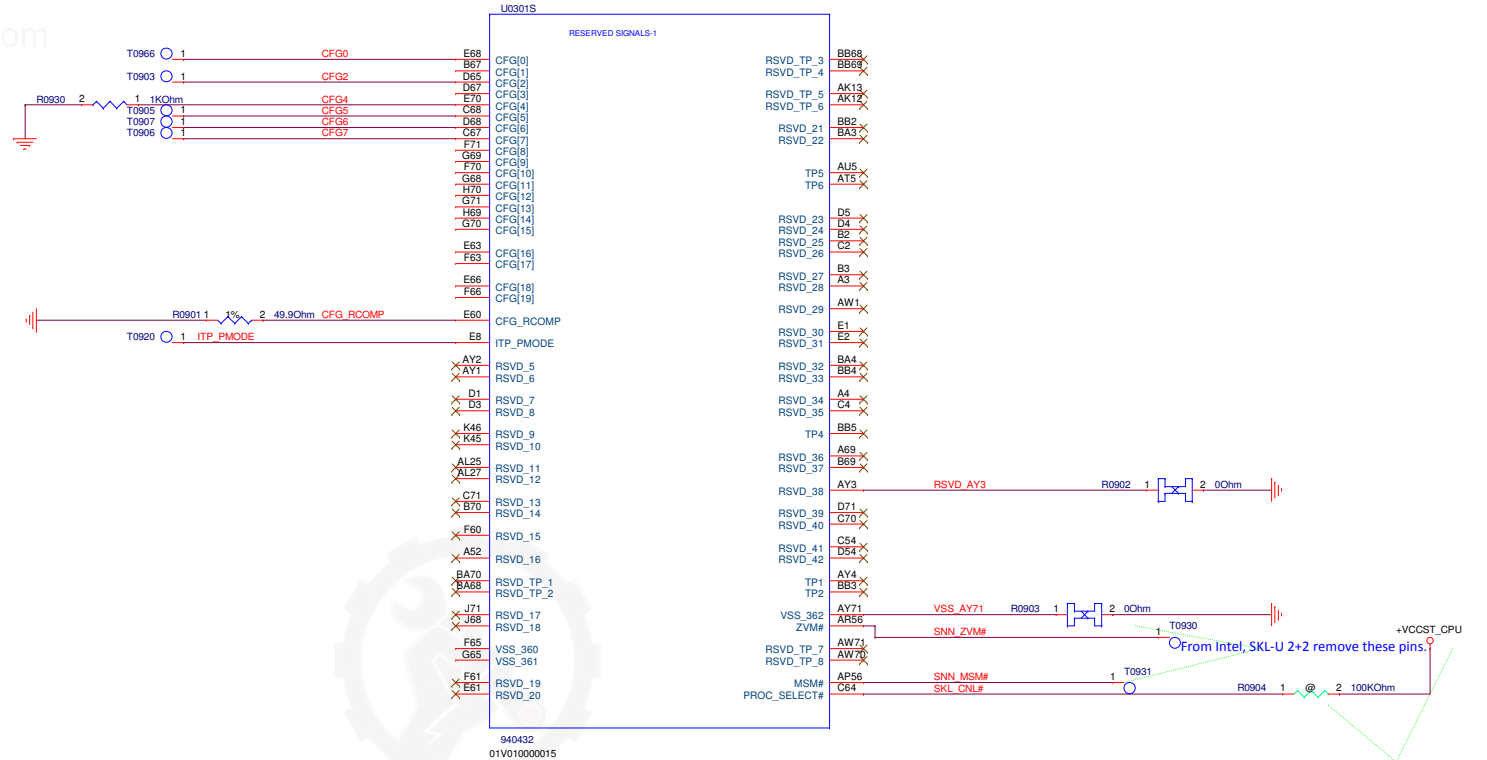


6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	Configuration Signals: The CFG signals have a default value of "1" if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. <ul style="list-style-type: none">CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted;<ul style="list-style-type: none">1 = (Default) Normal Operation; No stall;0 = Stall.CFG[1]: Reserved configuration lane.CFG[2]: PCI Express® Static x16 Lane Numbering Reversal.<ul style="list-style-type: none">1 = Normal operation0 = Lane numbers reversed.CFG[3]: Reserved configuration lane.CFG[4]: eDP enable;<ul style="list-style-type: none">1 = Disabled.0 = Enabled.CFG[6:5]: PCI Express® Bifurcation<ul style="list-style-type: none">00 = 1 x6, 2 x4 PCI Express*01 = reserved10 = 2 x8 PCI Express*11 = 1 x16 PCI Express*CFG[7]: PEG Training;<ul style="list-style-type: none">1 = (default) PEG Train immediately following RESET# de assertion.0 = PEG Wait for BIOS for training.CFG[19:8]: Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

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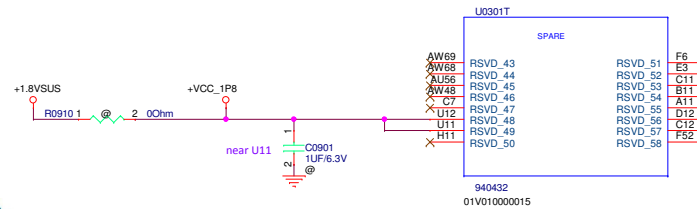
Intel confirm this pin is pulled high to +VCCST_CPU for CannonLake

1.3.2 [U] Skylake-U and Cannonlake-U Compatibility Decoupling Requirement

Two reserve pins (U11 and U12) for 1.8V were added to Skylake-U PCH to support Cannonlake-U PCH compatibility. For Skylake-U, the following changes will be made to Table 52-8 in the Skylake U/Y Platform Design Guide (IDP#543016).

Table 52-8 - Decoupling and Power Connection Requirement for Skylake-U PCH

Voltage Supply	Area	PCB Pin sharing power rail	Value	Size	Quantity	Placement (mm) (to Jdgo)	Place constraint(s) (to Jdgo)
V1.8A	VCCPGPF	AP16	-	-	-	-	-
	VCC1A5	AA1	1 uF	0402	1	E (x10 mm)	AA1
	VCC1A8	U13, U12	1 uF	0402	1	E (x10 mm)	U11, U12 (Note 1 & 5)



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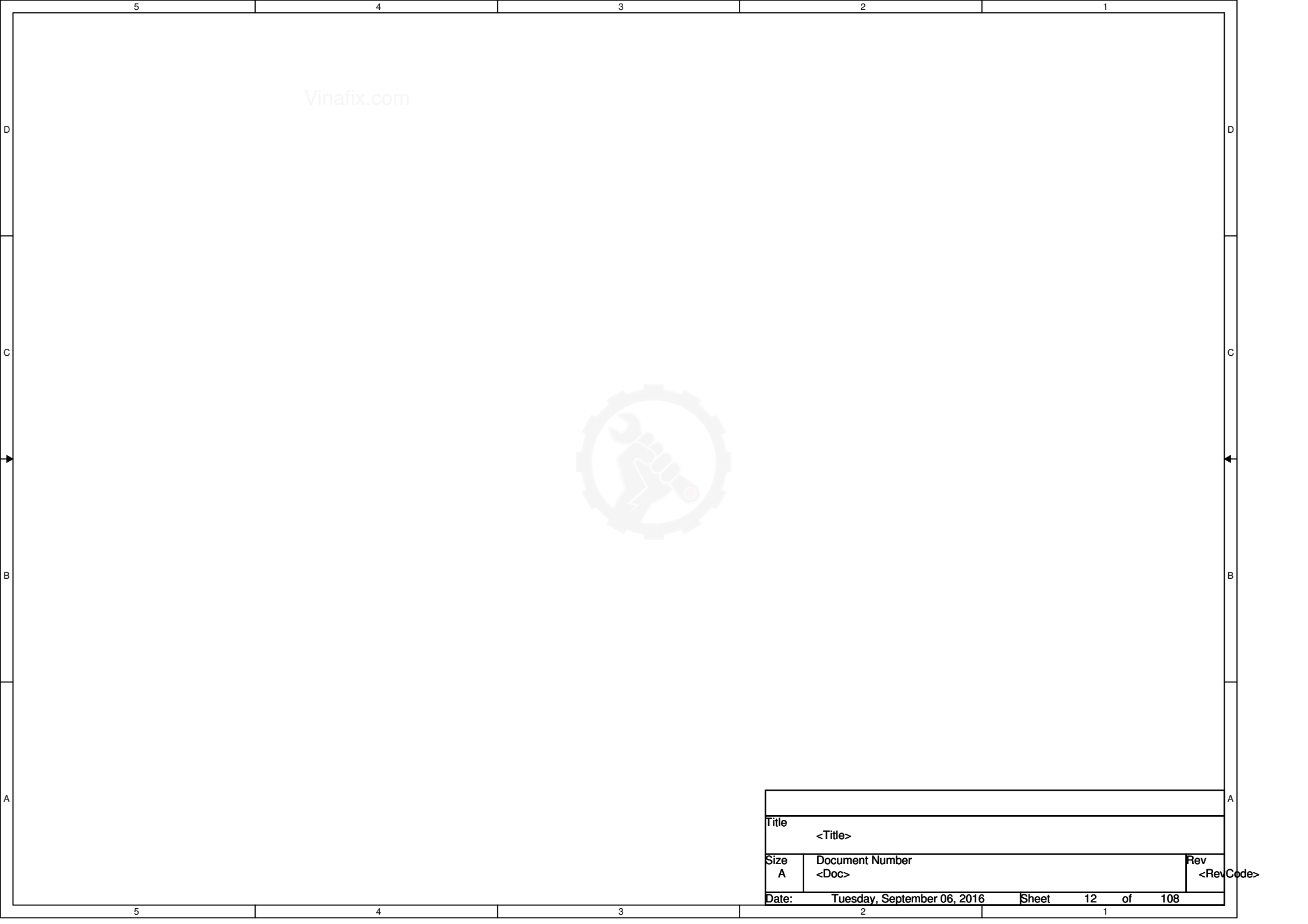
<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer:	
Size	100mm	Date	Rev
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<Variant Name>

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Engineer:	
Size	Rev. 1
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Date	Sheet



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Title <Title>			
Size A	Document Number <Doc>		Rev <RevCode>
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5

4

3

2

1

D

D

C

C |

B

B

A

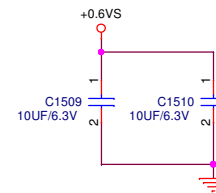
A

				A
Title <Title>				
Size A	Document Number <Doc>		Rev <RevCode>	
Date: Tuesday, September 06, 2016 Sheet 13 of 108				

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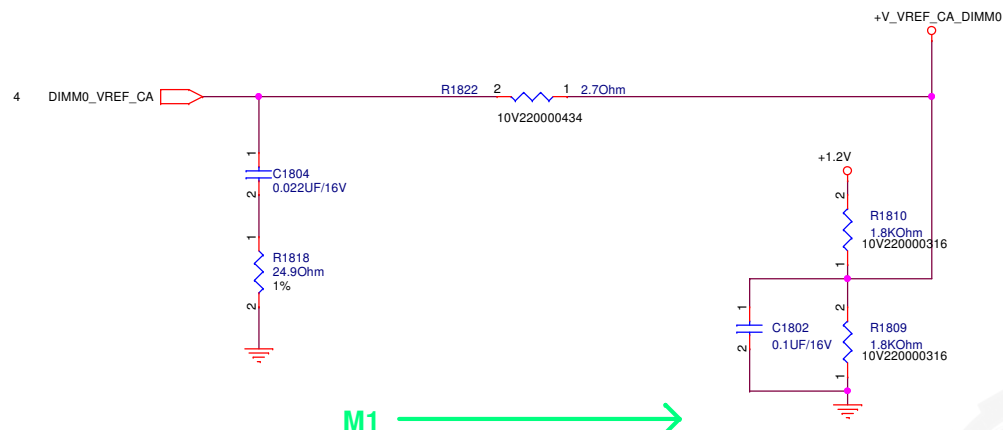
<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer:	
Size	Unit	Rev.	Rev. 1
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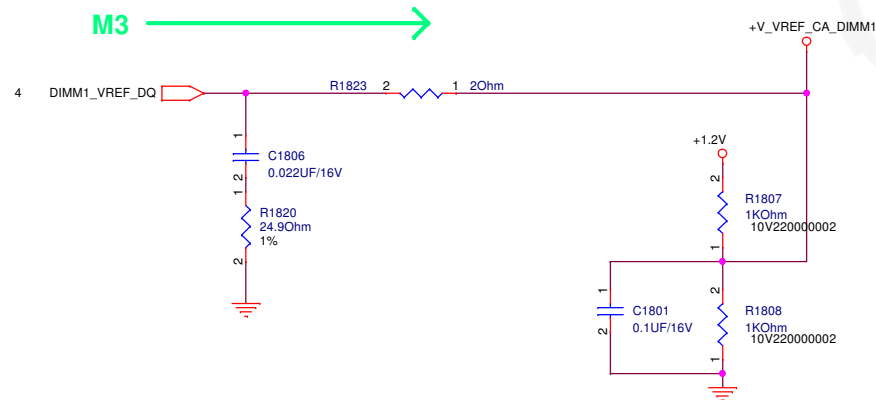
M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

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M3 →



M1 →



M1 →

+1.2V		+1.2V	4,7,15,16,17,57,83
+V_VREF_CA_DIMM0		+V_VREF_CA_DIMM0	16
+V_VREF_CA_DIMM1		+V_VREF_CA_DIMM1	17

Figure 4-46. SKL U DDR4/-RS x16 Devices Memory Down V_{REF-CA} Overview

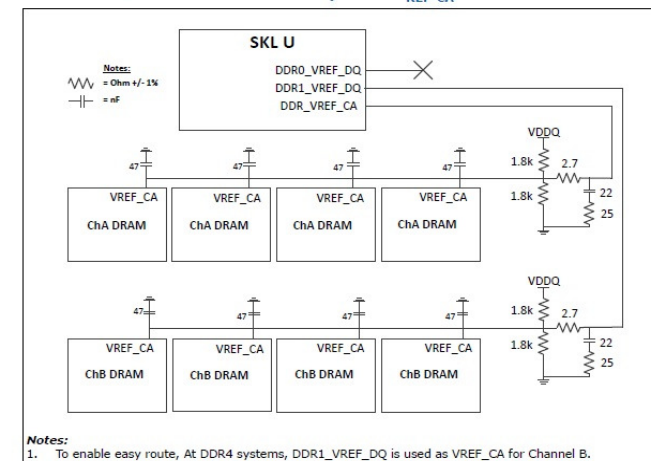
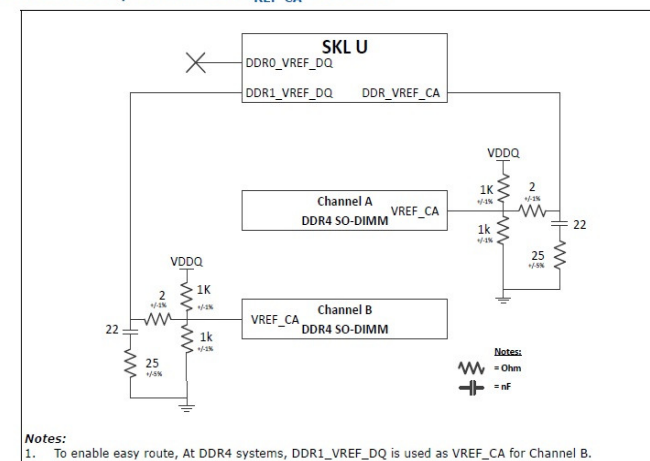


Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview

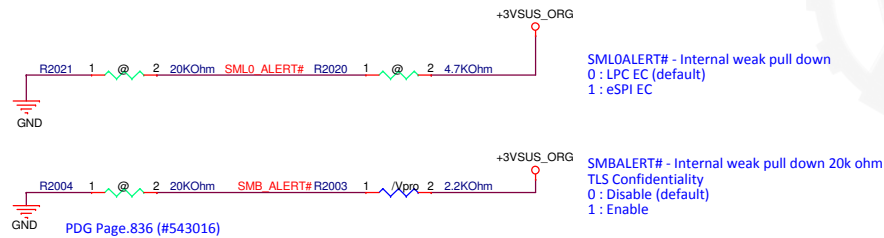
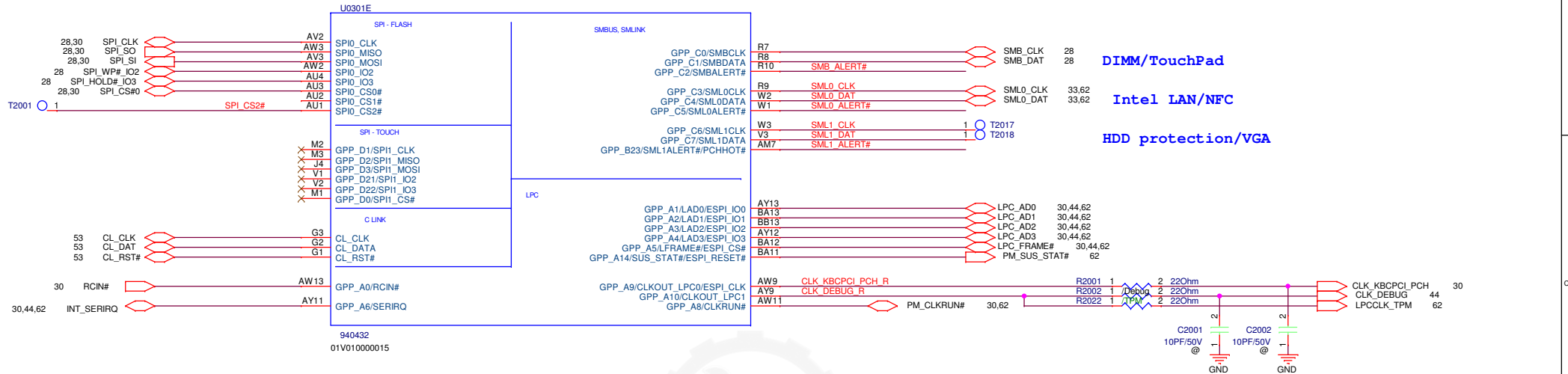


<Variant Name>

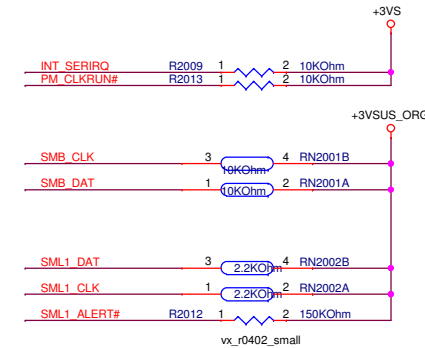
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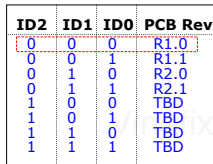
<Variant Name>			
PEGATRON Title :			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:			
Size	Project Name	Date	Rev. 1
	Tuesday, September 06, 2016	19	108
Date		Sheet	of



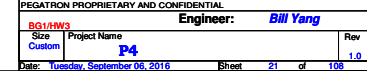
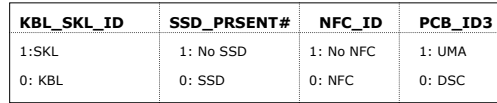
SMBALERT# / GPP_C2	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)</p> <p>1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.</p> <p>Notes:</p> <ol style="list-style-type: none"> The internal pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well.
--------------------	---------------------	------------------------	--

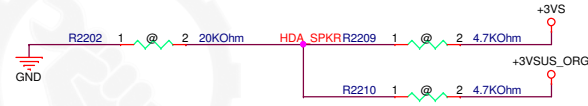
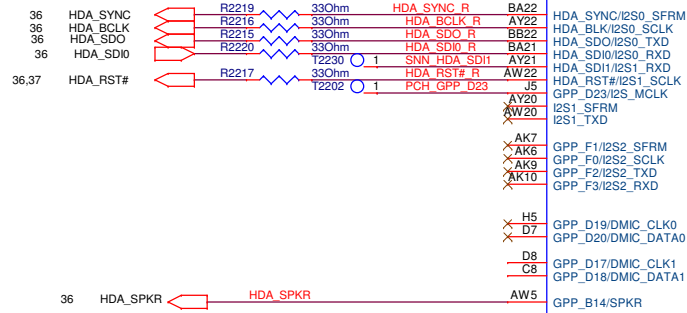
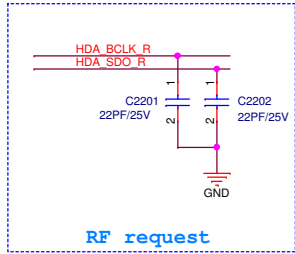


<Variant Name>



MEM_ID0	MEM_ID1	MEM_ID2	Memory Setting
0	0	0	SAMSUNG/K4A4G165WD-BCPB 4Gb 256Mb*16 0315-01C70PB
1	0	0	HYNIX/H5AN4G6NAFR-UHC 4G 256Mb*16 b0315-01EK0PB
0	1	0	SAMSUNG/K4A8G165WB-BCPB 8Gb 512Mb*16 0315-01HF0PB
1	1	0	HYNIX 8G
0	0	1	SAMSUNG/K4A8G165WB-BCRC 2400 512Mb*16 0315-01C80PB
1	0	1	SK HYNIX/H5AN8G6NAFR-UHC 2400 512Mb*16 0315-01W60PB
0	1	1	MICRON/MT40A512M16JY-083E:B 2400 512Mb*16 0315-01W90PB
1	1	1	DR4 2400 1Gb*16 1.2V FBGA96 MICRON/MT40A1G16WBU-083E:B 0315-01YC0PB





SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS_ORG



HDA_SDO - Internal weak pull down
FLASH_DESCRIPTOR SECURITY OVERRIDE
0 : Enable
30 1 : Disable

<Variant Name>

+3VS
+3VSUS_ORG

on MLB USB3.0

on MLB Type-C

on MLB USB2.0

On IO USB2.0/ON Swap Bay HUB

on MLB Type-C

on MLB Type-C

M.2 BT

Finger Printer

Normal Camera

SD

Touch Panel

USB3.0 with USB charge
USB2.0
Type-C

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U0301H

PCIE/USB3/SATA

SSIC / USB3

USB2

940432

01V010000015

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U

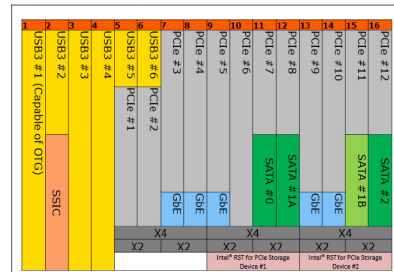


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express ⁴ Storage Devices	0	2	2
Notes: 1. USB 2.0 port numbers: 1-8 2. USB 2.0 port numbers: 1-10 3. USB 2.0 port numbers: 1-6 4. SATA Express Capable Ports (x2)			

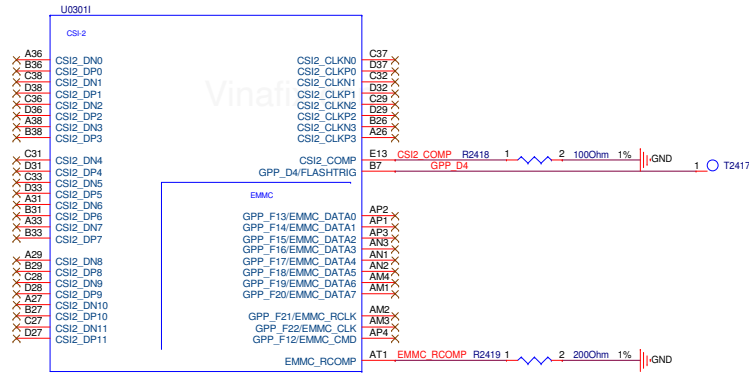
Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A
Premium-U	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	N/A
Premium-Y	USB 3.0 OTG	USB 3.0 SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	N/A

<Variant Name>

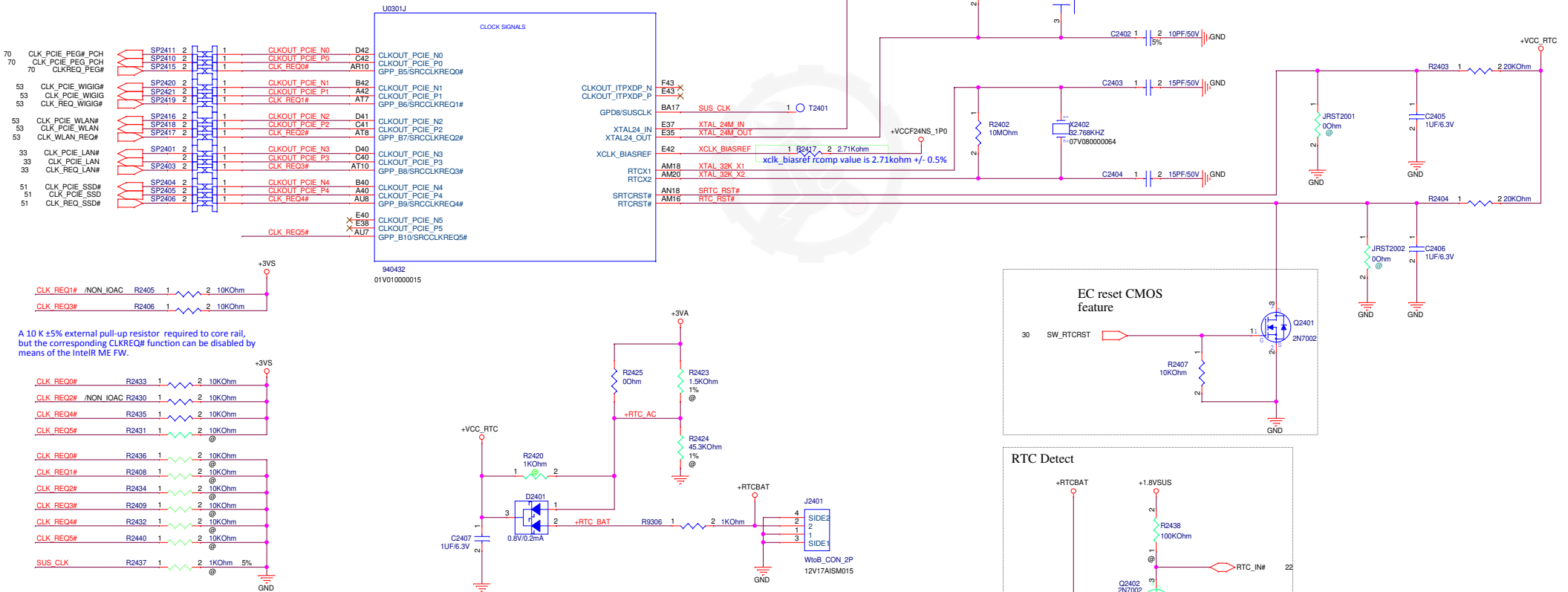
PEGATRON Title PCH(4)_PCIE,SATA,USB,
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Bili Yang**
BG1AHW3
Size Custom
Project Name **P4**
Date: **Tuesday, September 06, 2016** Sheet **23** of **108**
Rev **1.0**



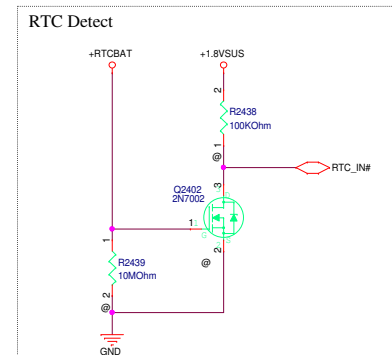
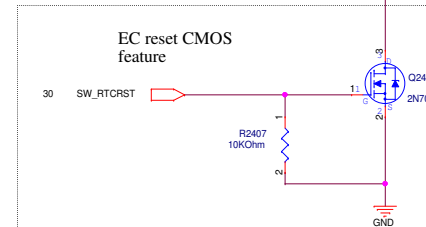
+VCCF24NS_1P0	+VCCF24NS_1P0	26
+VCC_RTC	+VCC_RTC	25,26,36,60
+AC_BAT_SYS	+AC_BAT_SYS	43,45,80,81,82,83,85,87,88
+3VS	+3VS	3,4,17,20,21,22,23,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+3VA	+3VA	30,31,36,41,43,53,55,57,67,81,88,93

24MHz signal 需包GND

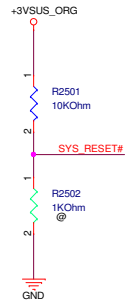


A 10 K $\pm 5\%$ external pull-up resistor required to core rail, but the corresponding CLKREQ# function can be disabled by means of the Intel ME FW.

If CLKREQ# control is not needed, say for a free running clock, do not pulldown signal to GND. This will increase leakage in Sx states.

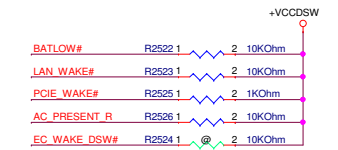
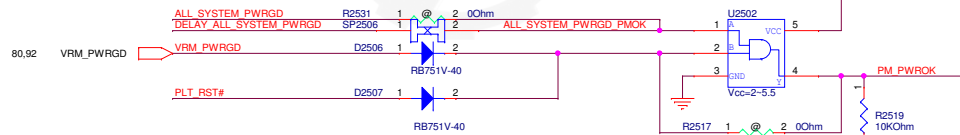
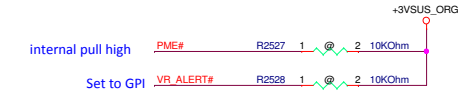
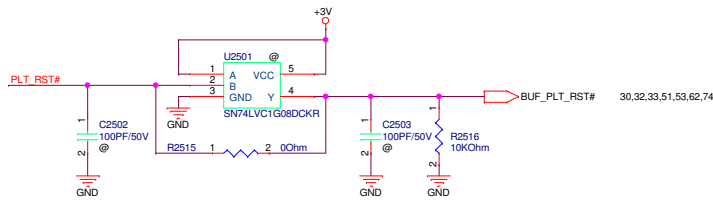
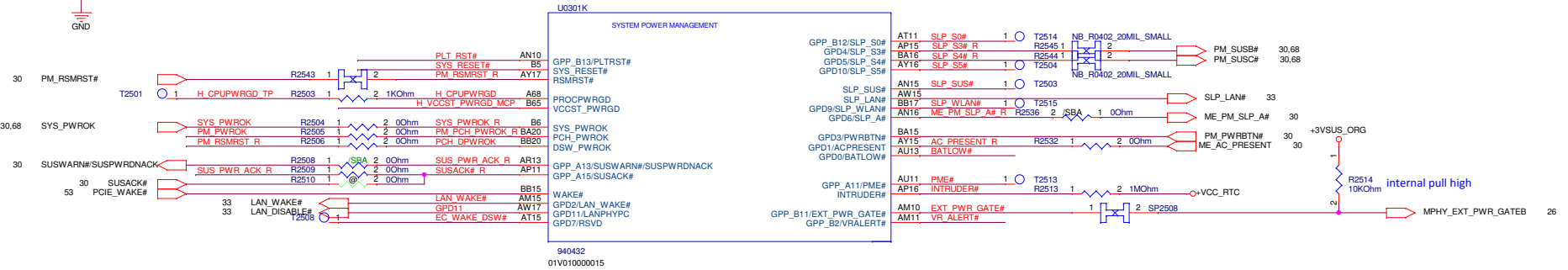


<Variant Name>

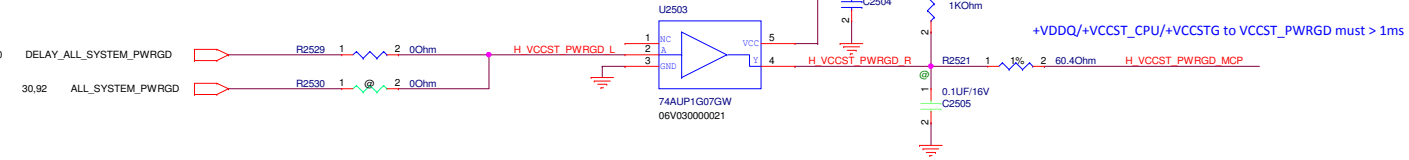


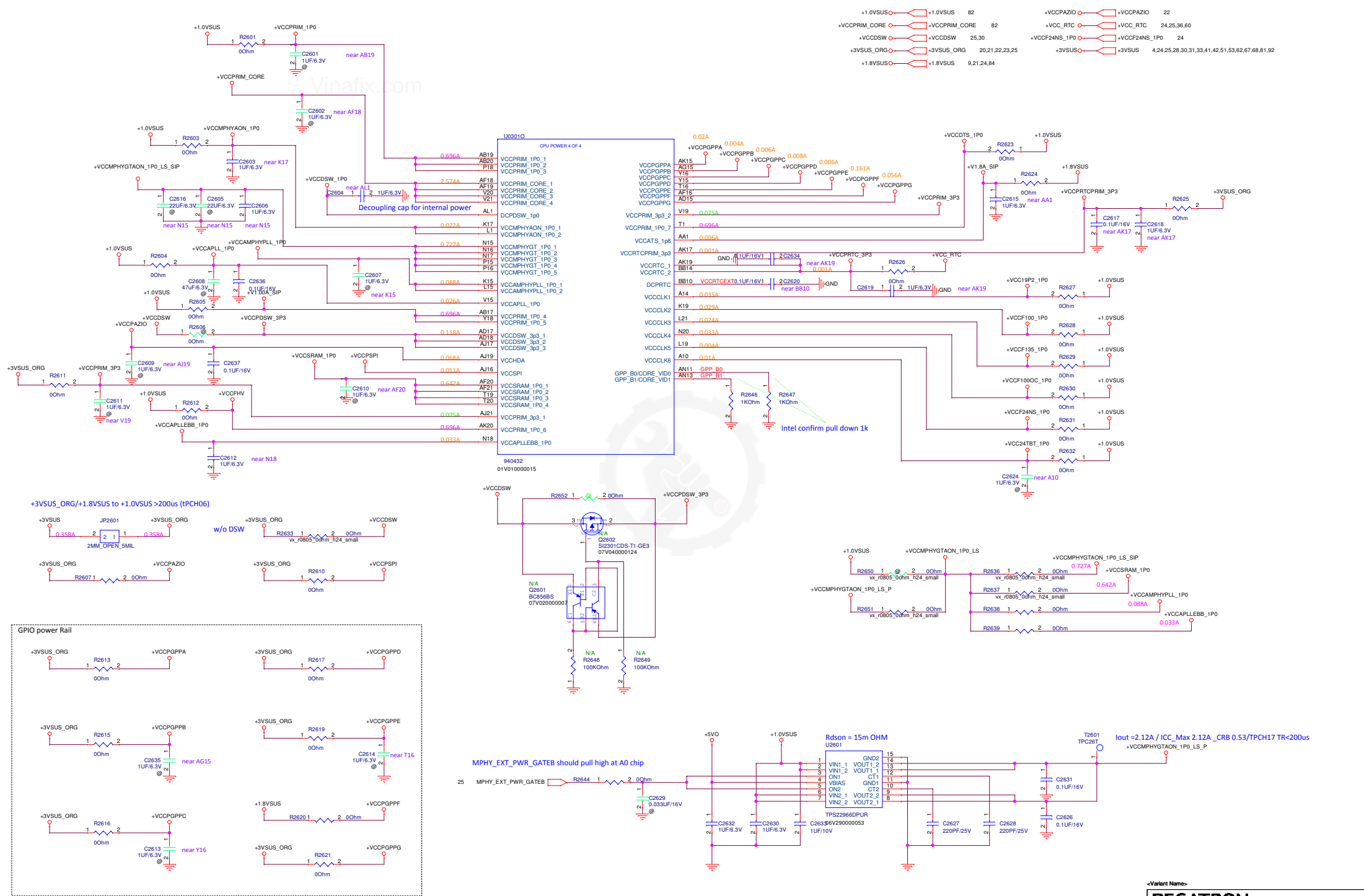
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+3VSUS		+3VSUS	4,24,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+VCCDSW		+VCCDSW	26,30
+3VSUS_ORG		+3VSUS_ORG	20,21,22,23,26
+3V		+3V	31,44,57,67,82,91
+VCC_RTC		+VCC_RTC	24,26,36,60
+VCCST_CPU		+VCCST_CPU	3,5,7,9



EC delay ALL_SYSTEM_PWRGD 2ms



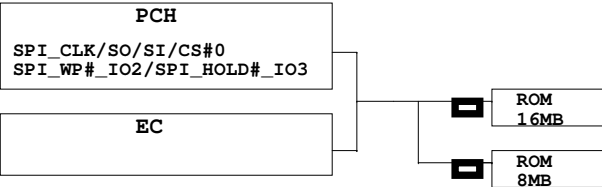
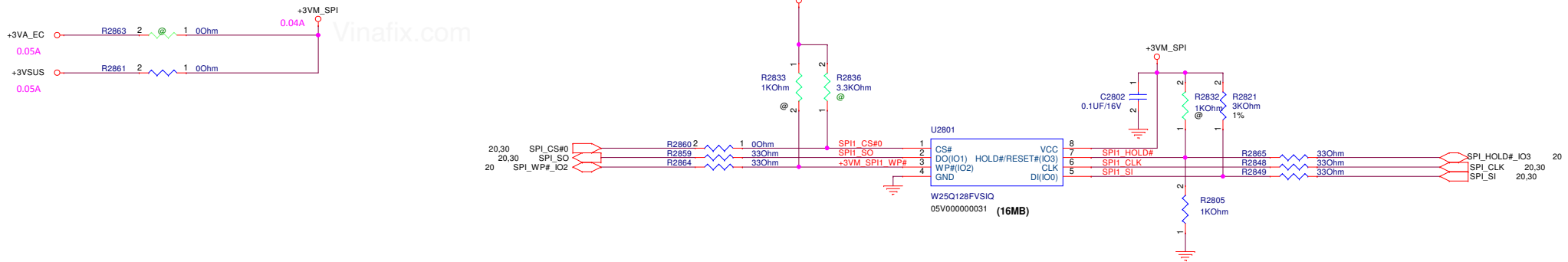


Vinafix.com

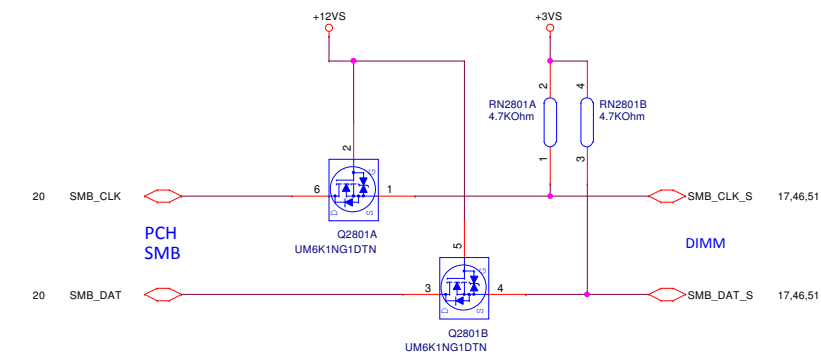


<Variant Name>			
PEGATRON Title :			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:			
Size	Project Name	Date	Rev. 1
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PCH SPI ROM



PCH SMBus

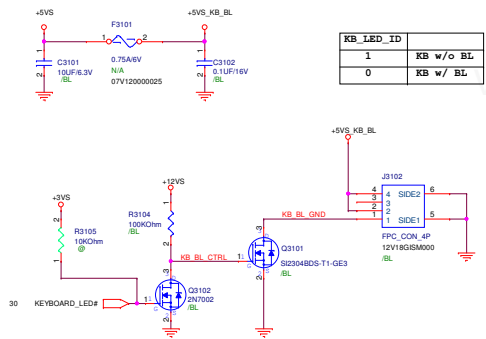


Vinafix.com

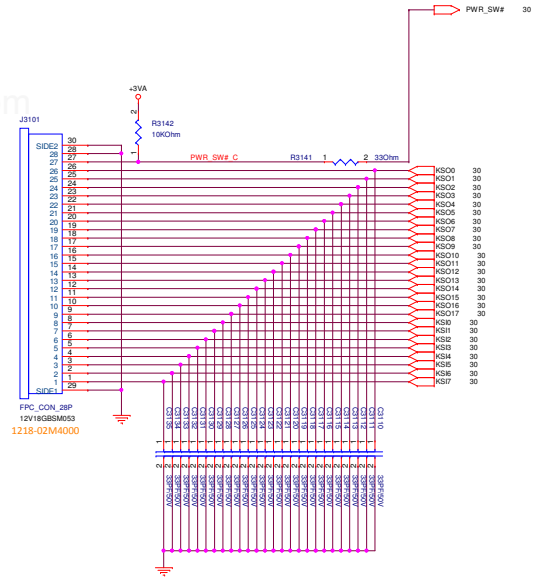


<Variant Name>		
PEGATRON Title :		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<Title> Engineer:		
Size C	Project Name KTKUG_25W	Rev 1.1
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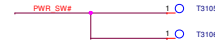
Keyboard LED







Keyboard

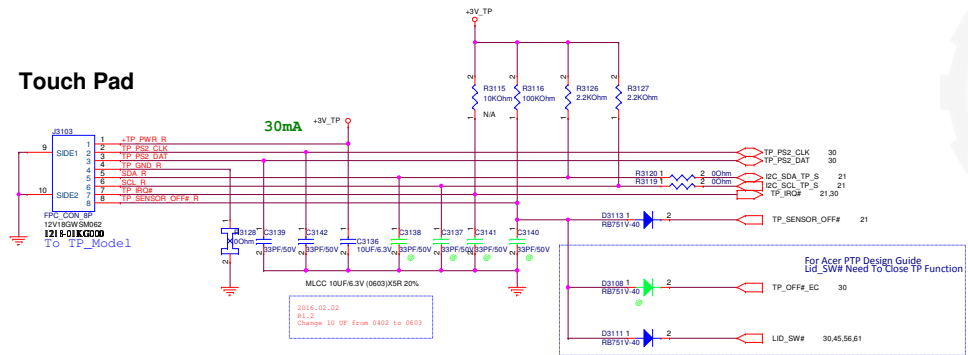


for Top/Bot side 各一 (開機測點) 6/2

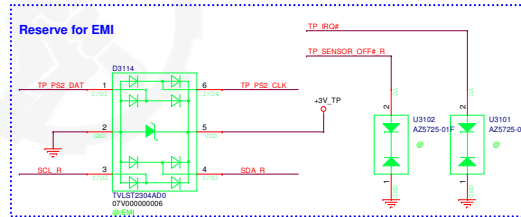


+5VS		+5VS	36,45,46,48,50,51,56,57,67,80,87,91
+3VS		+3VS	3,4,17,20,21,22,23,24,28,30,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+12VS		+12VS	28,57,62,91
+3V		+3V	25,44,57,67,82,91

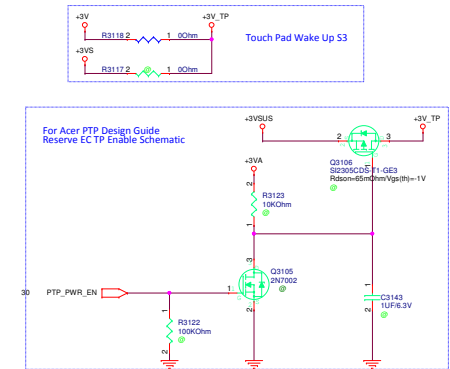
Touch Pad



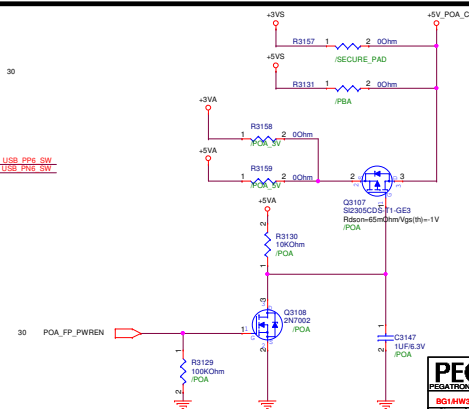
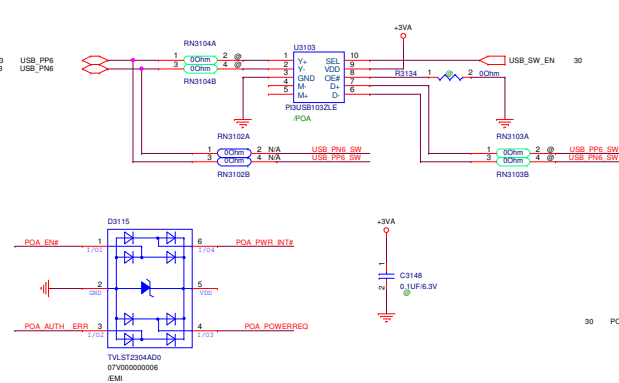
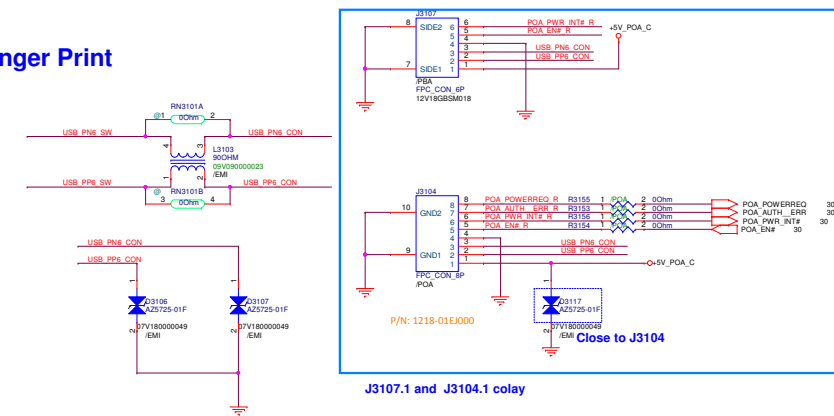
- Reserve for EMI



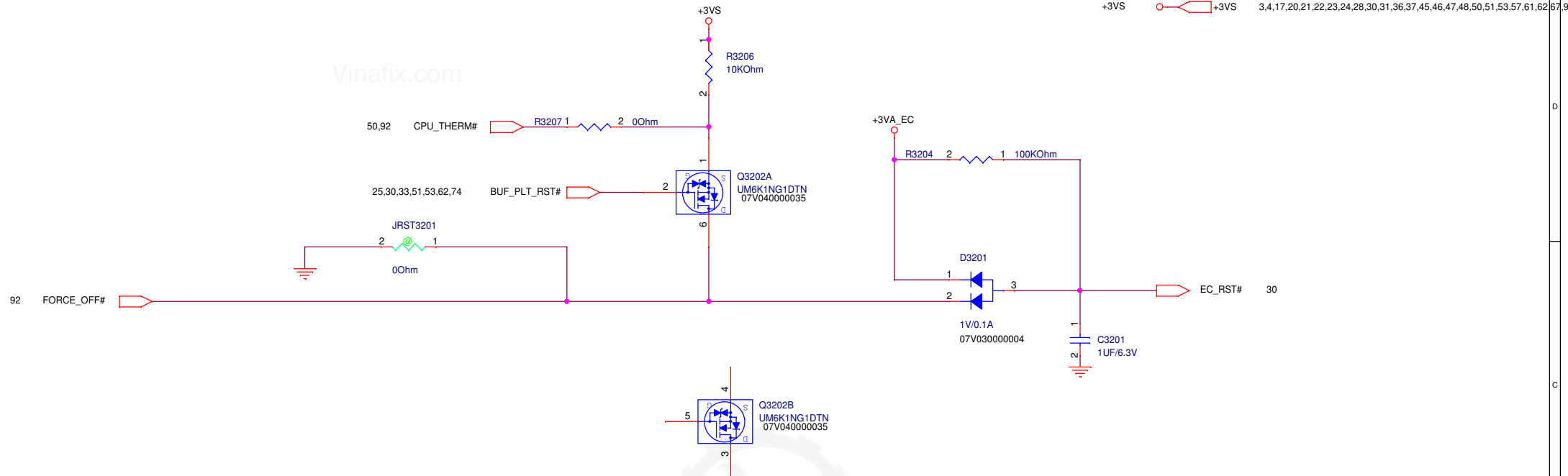
For Acer PTP Design Guide
Reserve EC TP Enable Schematic



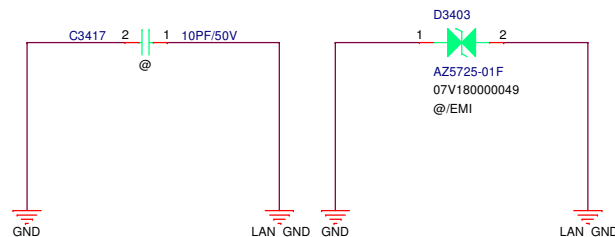
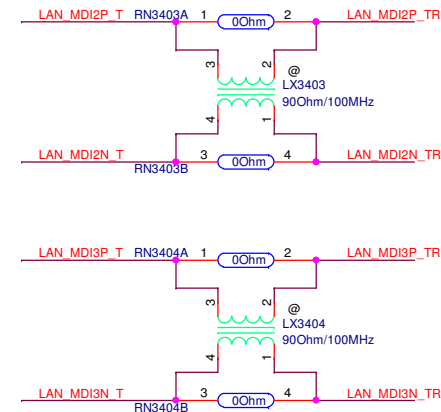
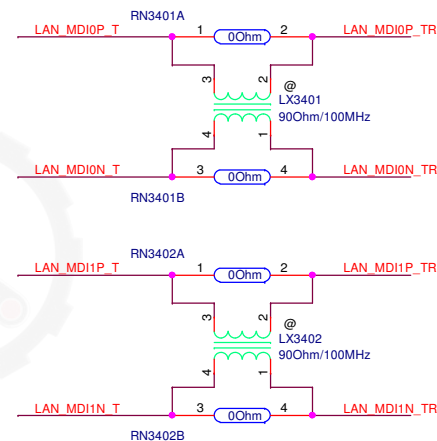
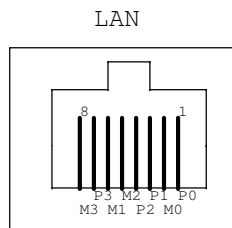
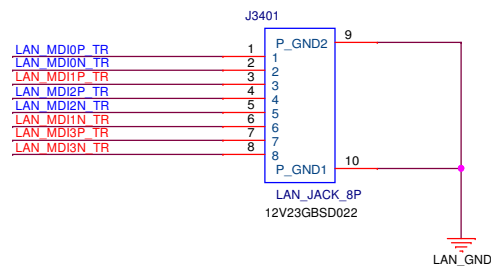
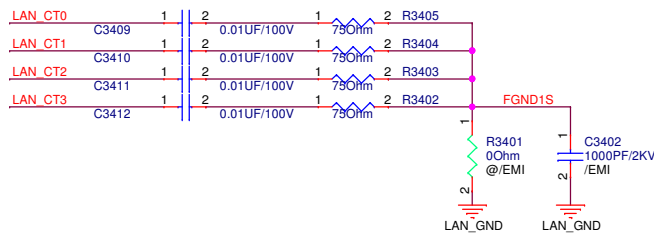
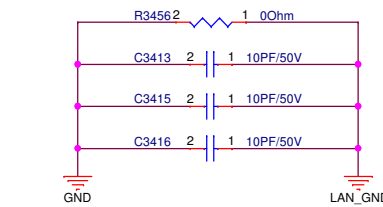
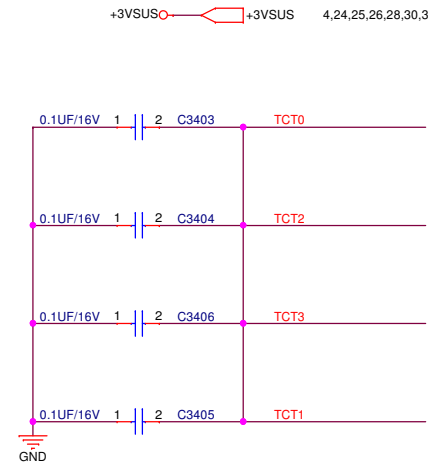
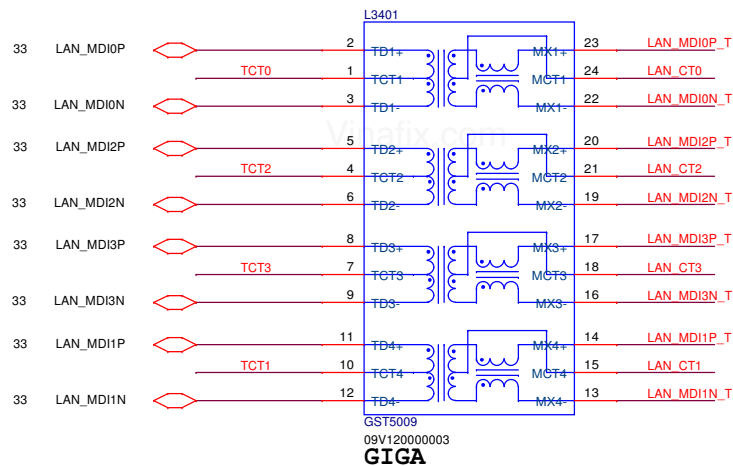
Finger Print



Vinafix.com



Remove 10s RTC reset



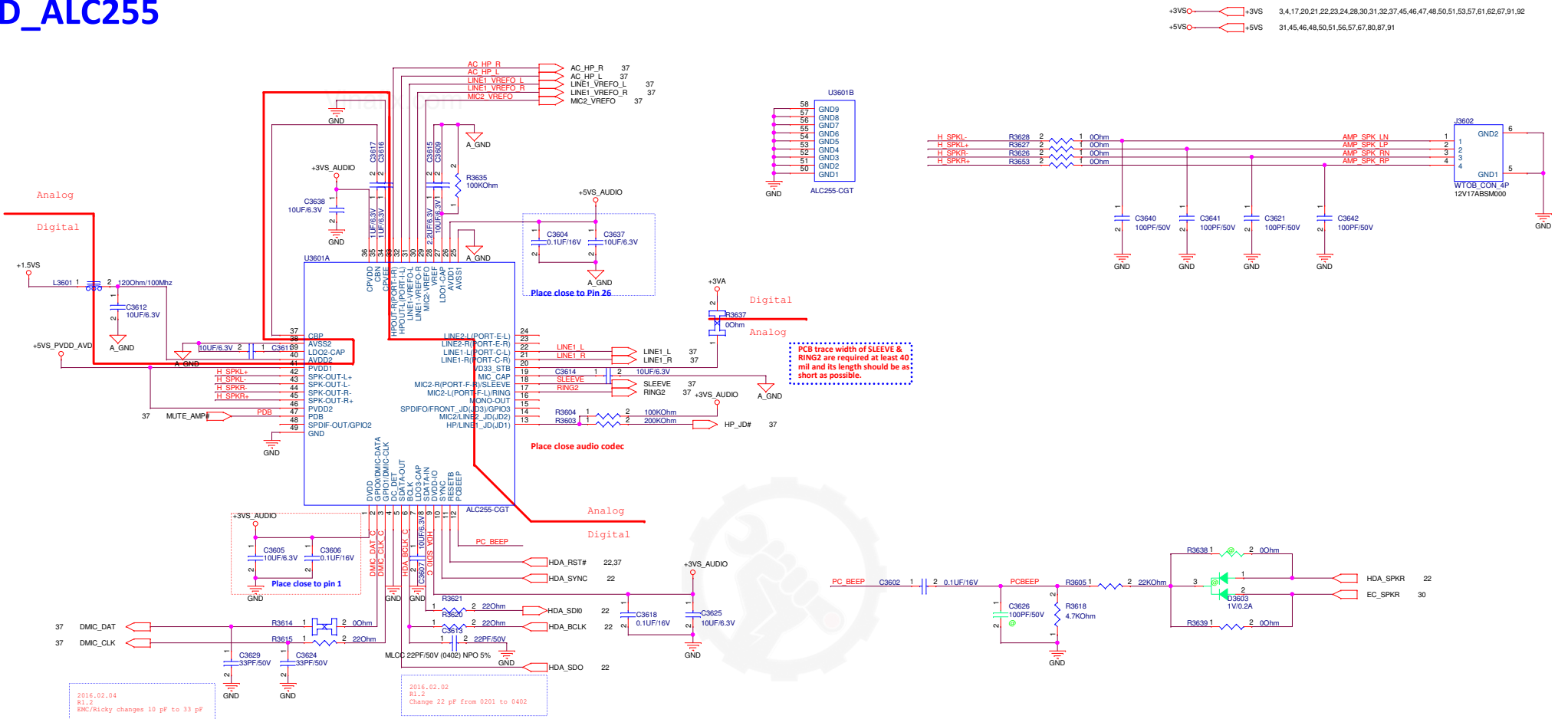
Place near chassis GND

Vinafix.com



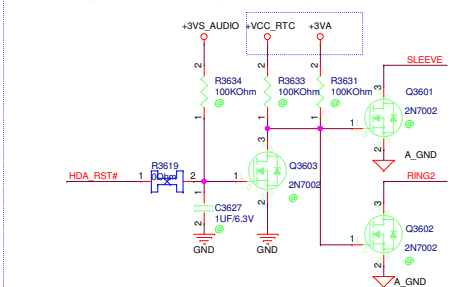
<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name KTRUG_25W	Rev 1.1	
Date: Tuesday, September 06, 2016		Sheet 35 of 108	

AUD_ALC255

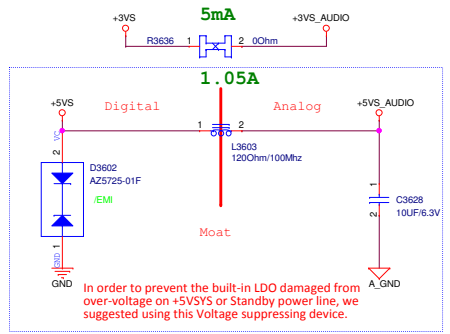
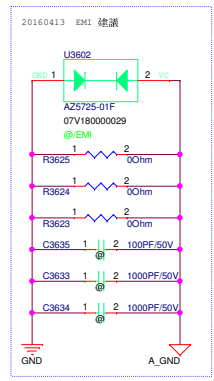


<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTEH High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

Grounding circuit for combo jack SLEEVE pin

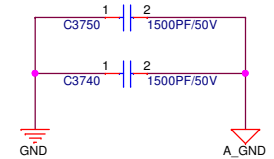
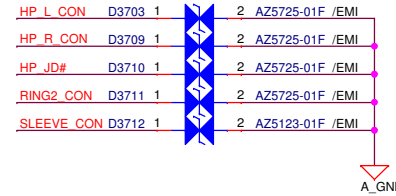
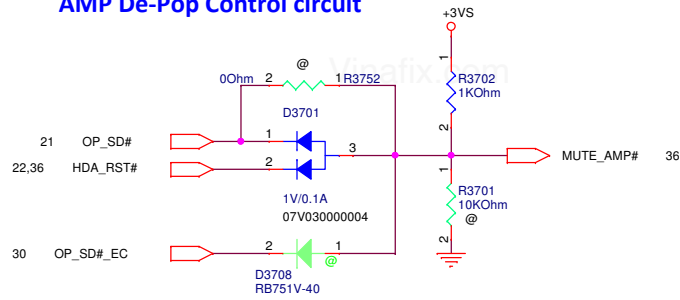


To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

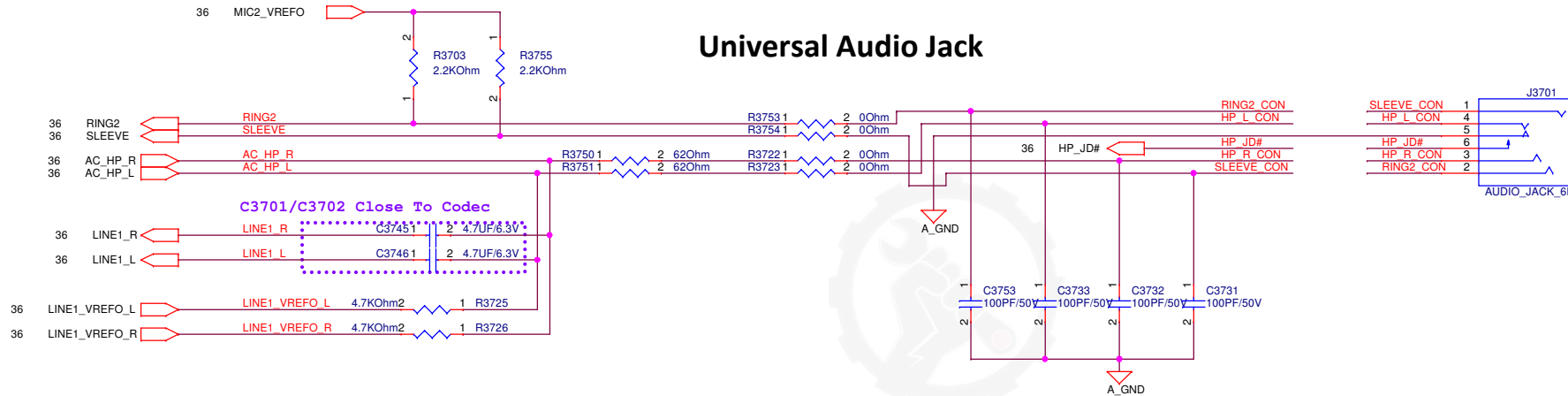


2015.12.07
R1.1
EMI build confirm

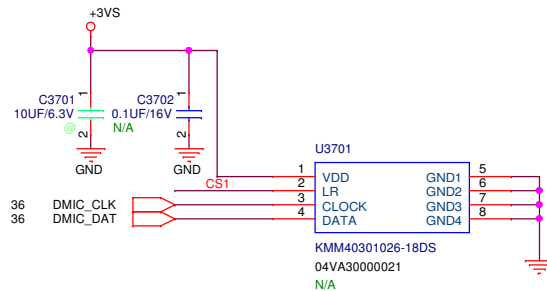
AMP De-Pop Control circuit



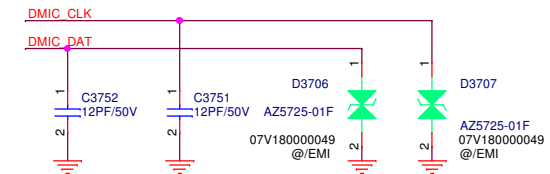
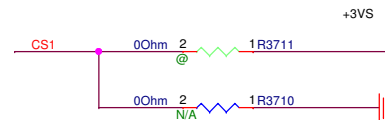
Universal Audio Jack



DMIC



Single MIC	Left Channel	Right Channel
CS Pin	Pull Down	Pull Up



<Variant Name>

Vinafix.com

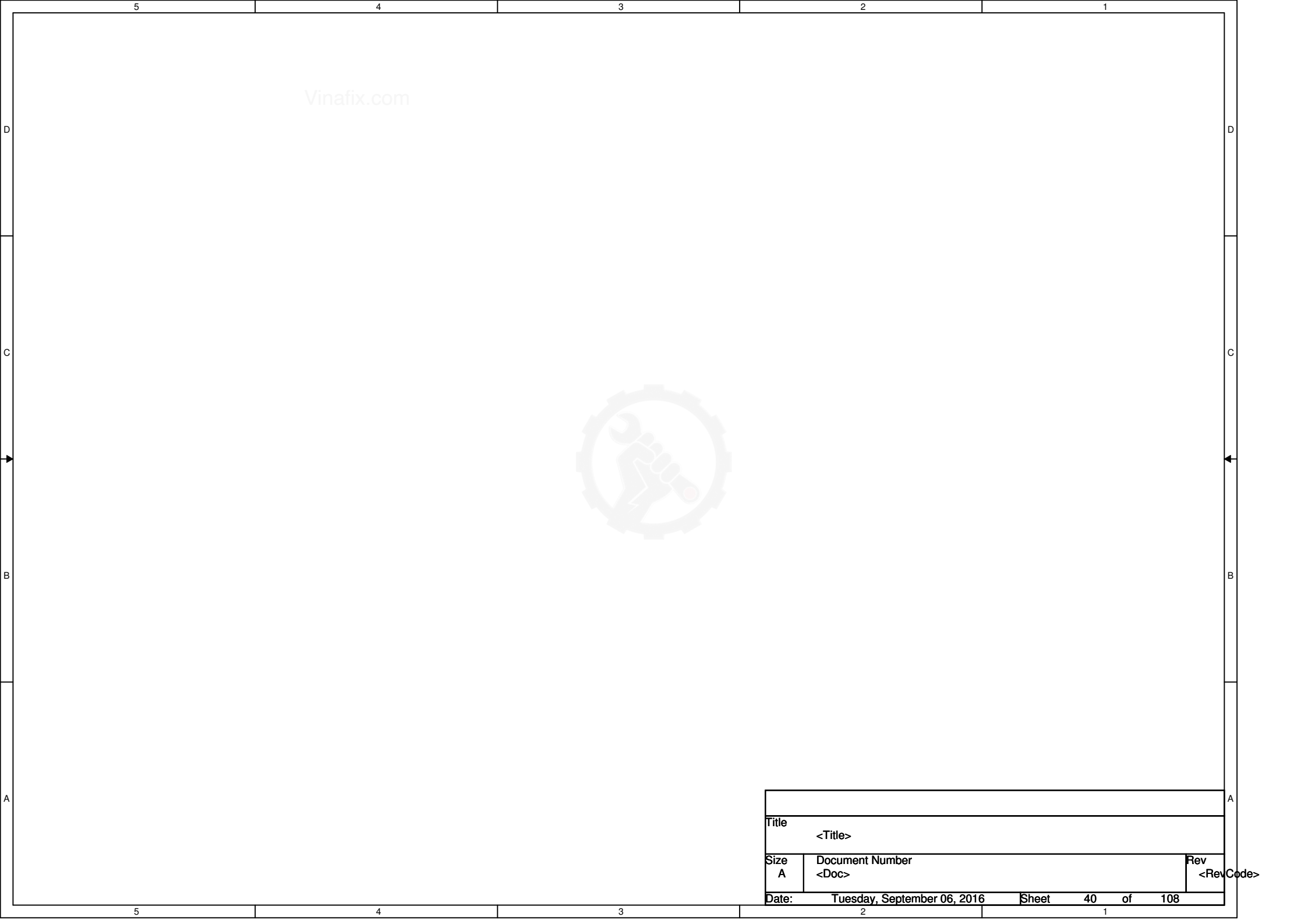


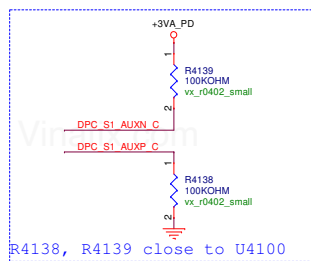
<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name KTRUG_25W	Rev 1.1	
Date: Tuesday, September 06, 2016		Sheet 38 of 108	

Vinafix.com



<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name KTRUG_25W	Rev 1.1	
Date: Tuesday, September 06, 2016		Sheet 39 of 108	





V5_VCONN

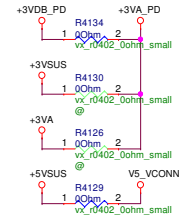
1

2

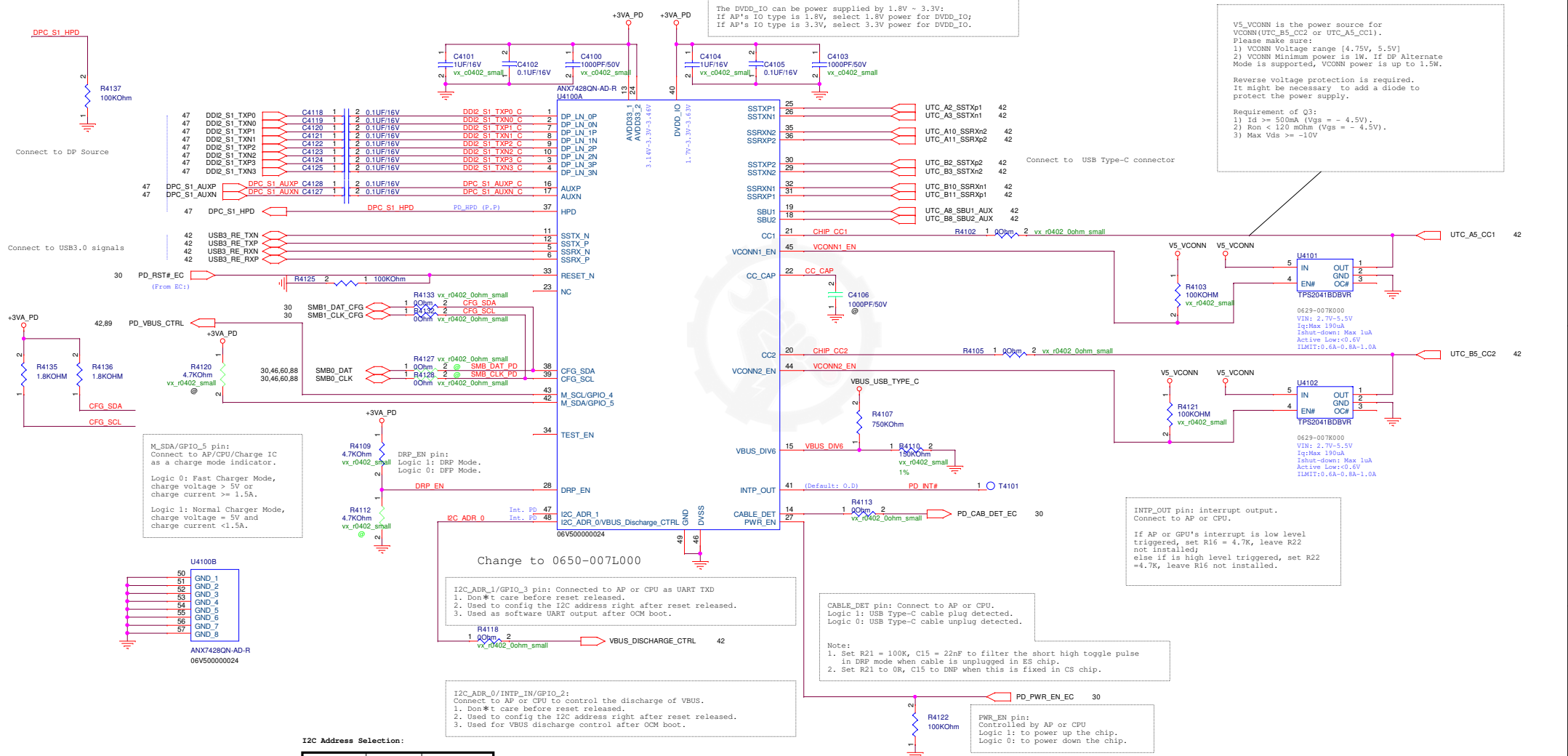
C4126
10UF/6.3V

@

The diagram shows a vertical wire with a red circle at the top labeled 'V5_VCONN'. Below it is a green capacitor symbol labeled 'C4126' and '10UF/6.3V'. The bottom of the capacitor is connected to a ground symbol. A circled '@' symbol is located to the right of the capacitor.



VBUS_USB_TYPE_C	VBUS_USB_TYPE_C	42,43
+3VA	+3VA	24,30,31,36,43,53,56,57,67,81,88,93
+3VA_PD	+3VA_PD	42
+3VSUS	+3VSUS	4,24,25,26,28,30,31,33,42,51,53,62,67,68,81,92
+3VDB_PD	+3VDB_PD	43



I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

12C_ADR_1 and 12C_ADR_0 pins:

- 1. The 12C address is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
- 2. There are internal pull-down resistors on 12C_ADR_0 and 12C_ADR_1 pins.
- 3. If external pull-up resistor is not populated, the 12C_ADR_0 or 12C_ADR_1 is logic 0.
- 4. If external pull-up is populated, the 12C_ADR_0 or 12C_ADR_1 is logic 1.

Optional:
If PMIC can detect VBUS presence and disable/enable VBUS,
the VBUS control circuit can be removed.

Requirement of the PMOSFETs U9600 and U9601:

- 1) Max Vds >= -30V.
- 2) Max Vgs >= +/-25V.
- 3) Id >= 5A.
- 4) Ron < 100 mΩm (Vds = -4.5V, Id = -5A).

VBUS_CTRL	5V VBUS Output	5-20V VBUS Charge Input
Logic 0	Disable	Enable
Logic 1	Enable	Disable

VBUS_USB_TYPE_C

U4201
AC84805
07V040000175
07C4-C3F8000

+USB_PD_IN

Note:
1. If battery charger can operate with 5V input, no more circuits are needed.
2. If battery charges needs higher voltage than 5V to operate correctly, ANX74xx should be powered by VBUS and local power.

R4205 10K
Q4201 N7602AK
07V040000000

VBAT

R4204 100K
Q4204 N7602AK
07V040000000

Requirement of NMOSFET Q9604:
 $I_{DS} = I_{BATT} \approx 1A$
 $V_{GS}(min) < 1V$
If need PD output 20VMAX, VGS>=3V

[illegible]

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

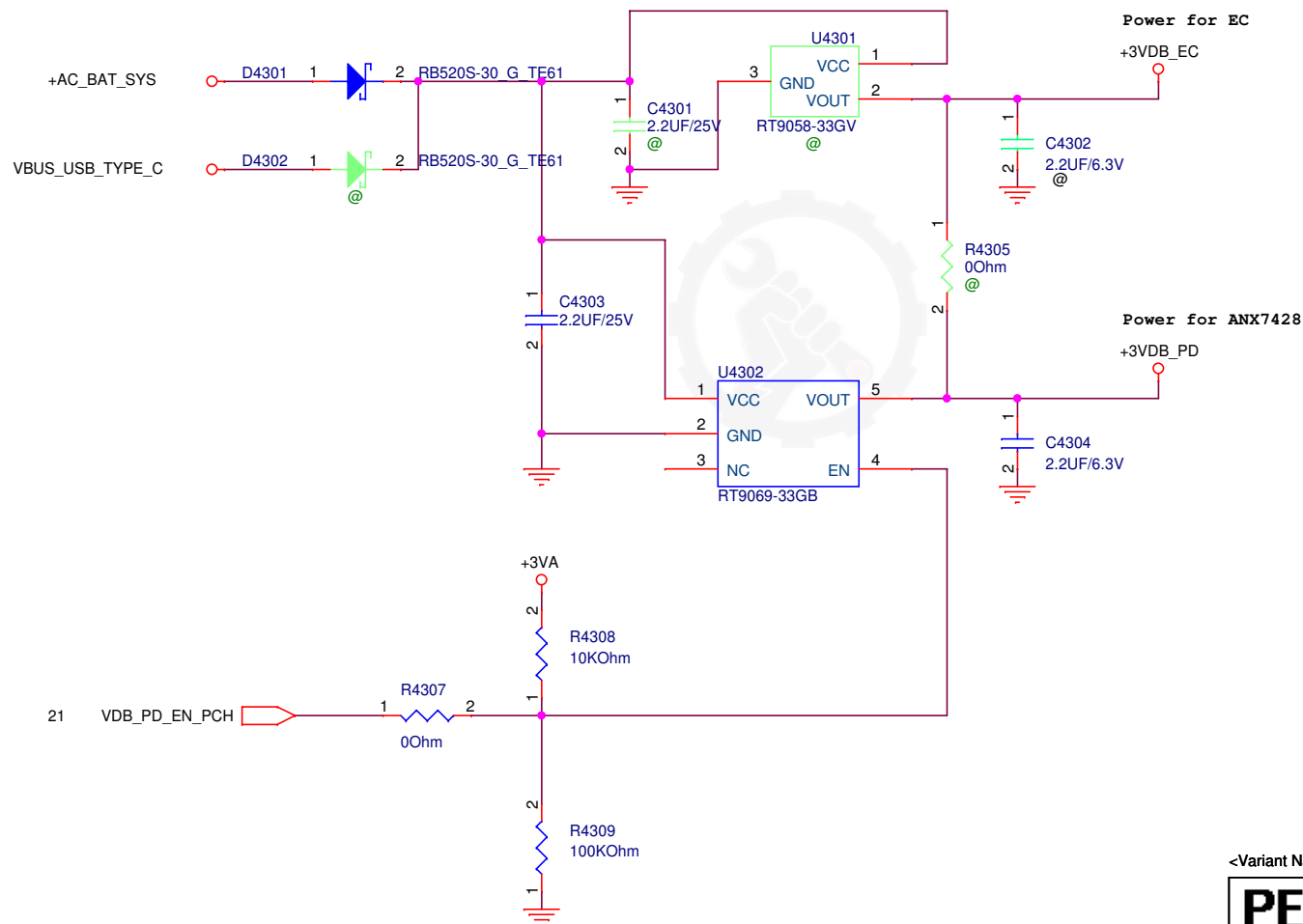
PEGATRON		Title: USB Type-C Receptacle	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		Bill Yang	
Size Custom	Project Name P4	Rev 1.0	
Date:	Tuesday, September 06, 2016	Sheet	42 of 108





Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

Requirement of U1:

- 1) Vin range: 4V-30V.
- 2) Vout: EC's operating voltage + Vf of D1
- 3) Output current \geq EC's operating current.



VBUS_USB_TYPE_C		VBUS_USB_TYPE_C	41,42
+AC_BAT_SYS		+AC_BAT_SYS	45,80,81,82,83,85,87,88
+3VDB_EC		+3VDB_EC	30
+3VDB_PD		+3VDB_PD	41

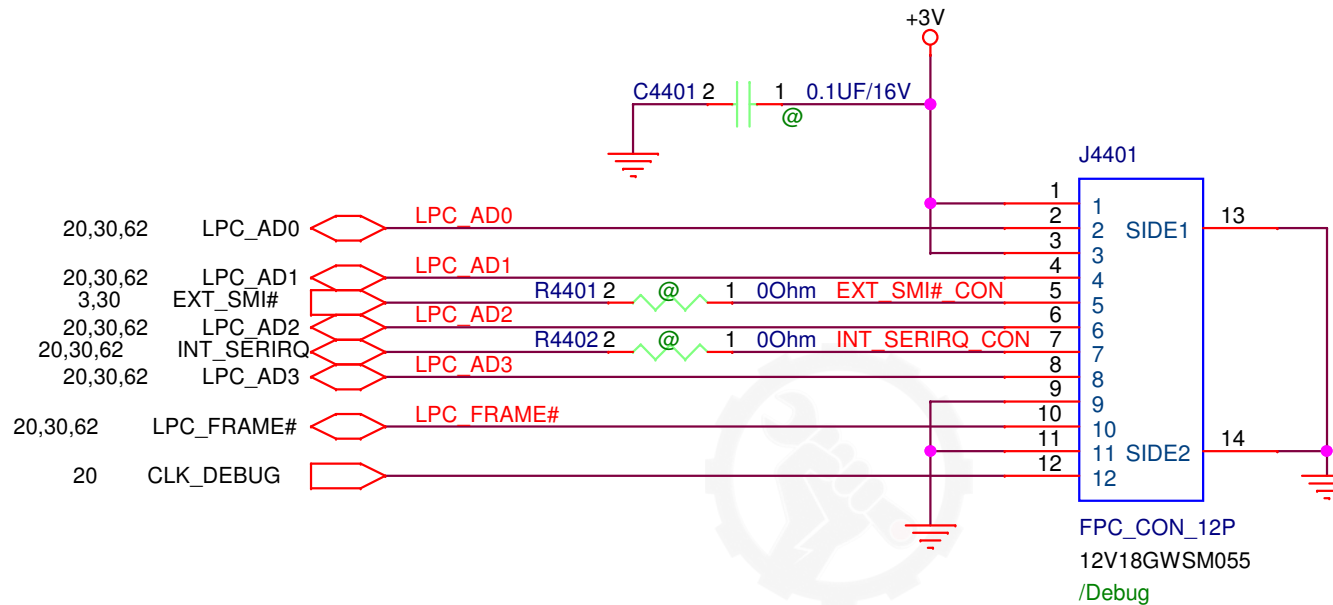
<Variant Name>

PEGATRON Title : **Dead Battery**
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Bill Yang**

Size Custom	Project Name P4	Rev 1.0
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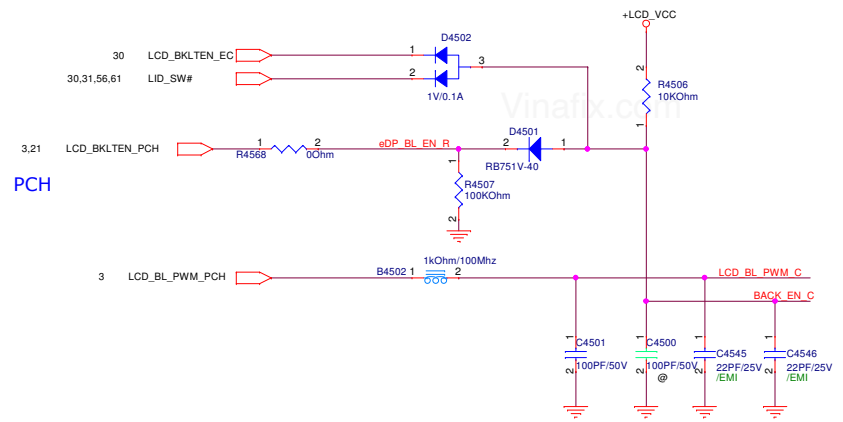
Date: Tuesday, September 06, 2016 Sheet 43 of 97



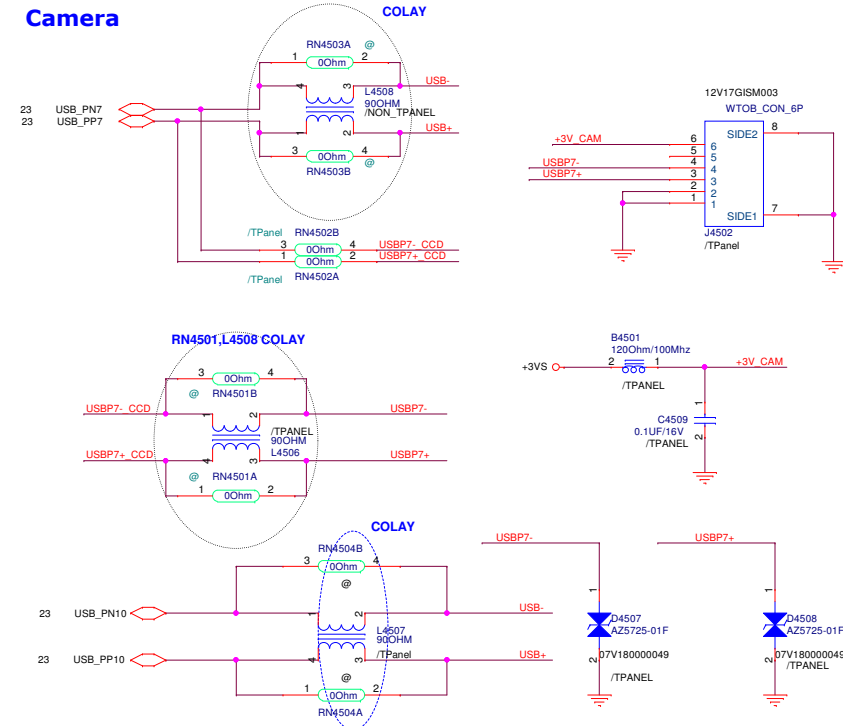
<Variant Name>

PEGATRON		Title : BUG_Debug	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Bill Yang	
Size Custom	Project Name P4		Rev 1.0
Date: Tuesday, September 06, 2016		Sheet 44 of 108	

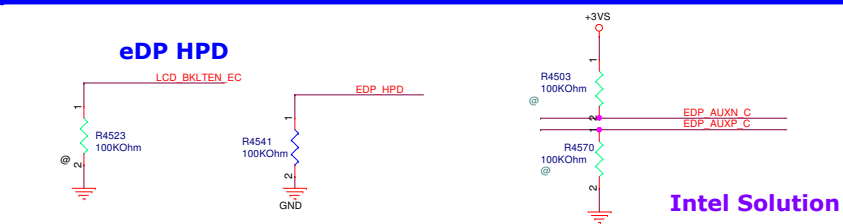
Controller circuit



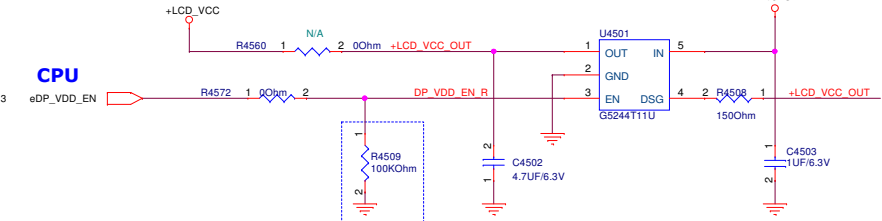
Camera



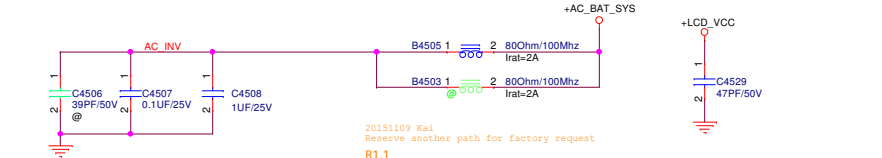
eDP HPD



LCD_VCC for eDP

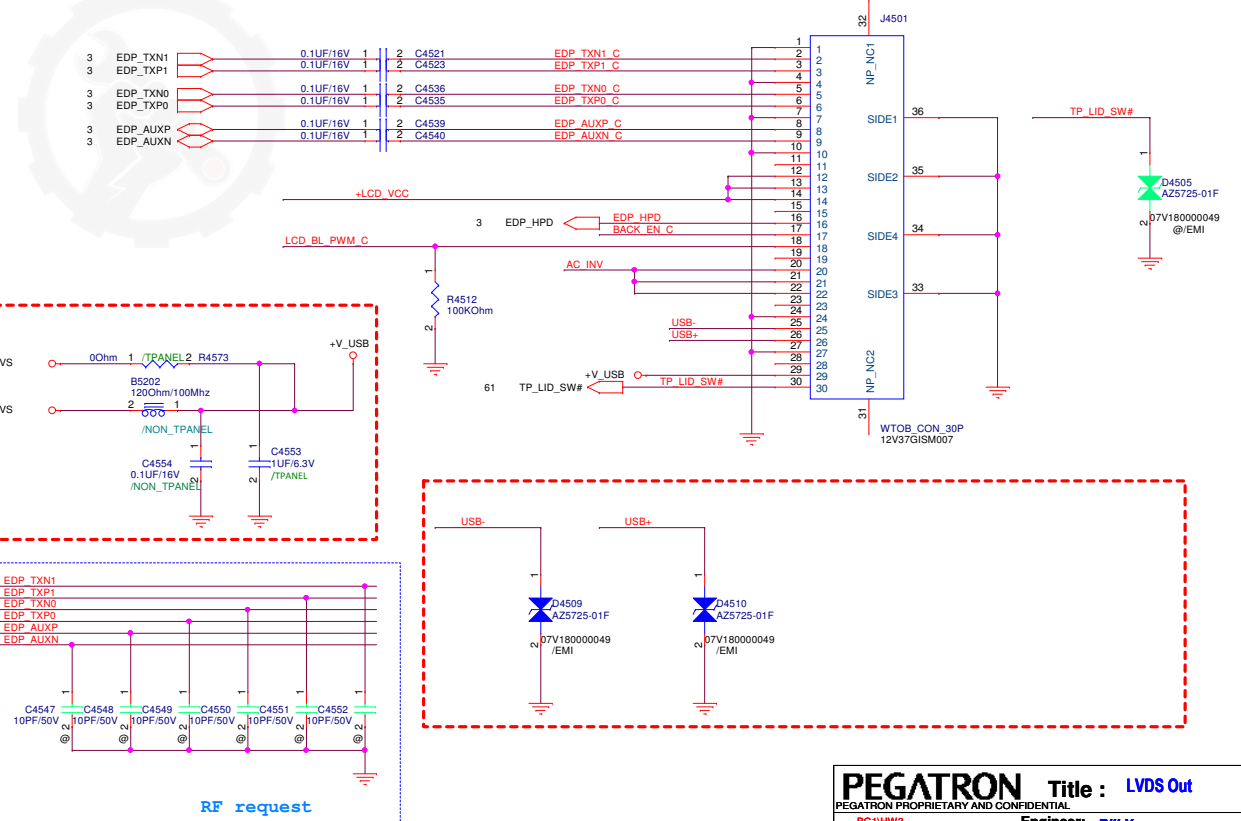


Check PCH/FCH or CPU PD

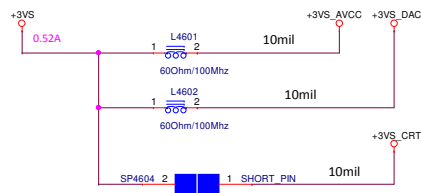


eDP Connector

NOTE:
Entire trace of Panel_VCC & LCD_VCC should be wider than 80-mil

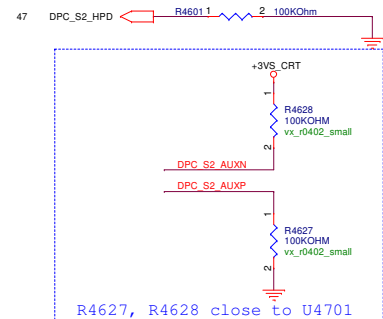
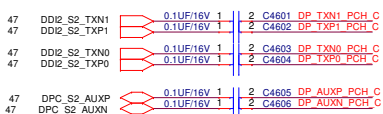


Power



CPU Interface

DP main link total length < 8 inch
VIA < 2



DP2VGA Realtek RTD2166

Rom / Flash Mode :

		POL1 (Pin10)	
		0	1
POL2 (Pin9)	0	No Use	No Use
	1	(V) Rom mode	Ext Flash mode

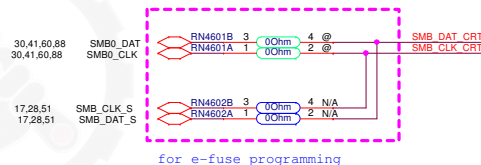
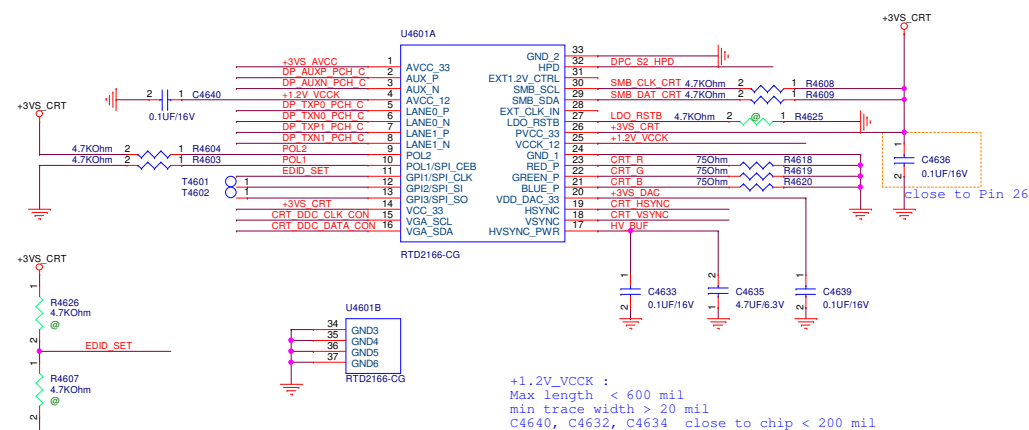
Embedded EDID setting :

EDID_SET (Pin11)	Mode
0 or NC	(V) Disable RTD2166 Embedded EDID
1	Enable RTD2166 Embedded EDID

LDO Mode :

LDO_RSTB (Pin27)	Mode
1 or NC	(V) embedded LDO Mode
0	External 1.2V Mode

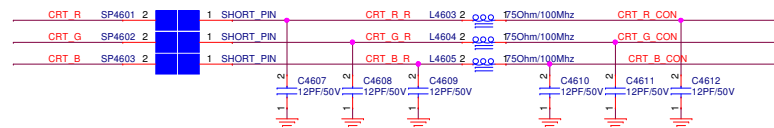
1: Pull High 0: Pull Down



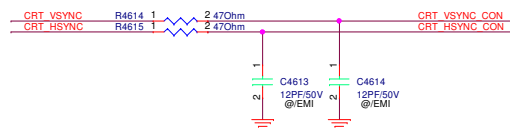
```
CRT_HV Sync Voltage setting :
R4605 : 5V
R4606 : 3.3V
```



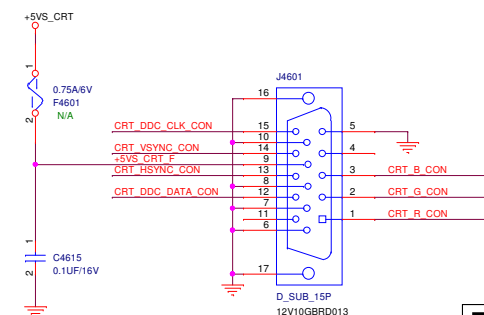
Max mismatch between RGB signal < 200 mil,
total trace length < 6 inch

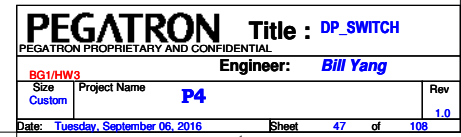


CRT_HV Sync total trace length < 6 inch



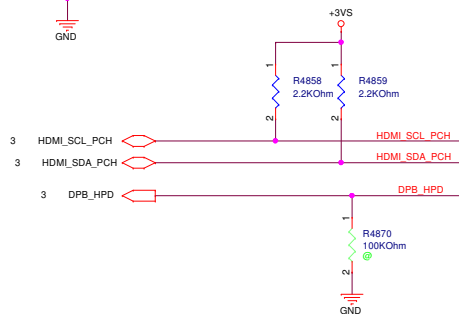
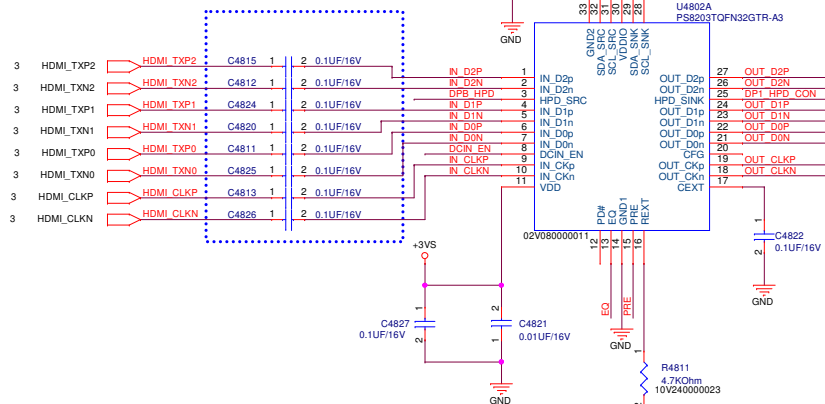
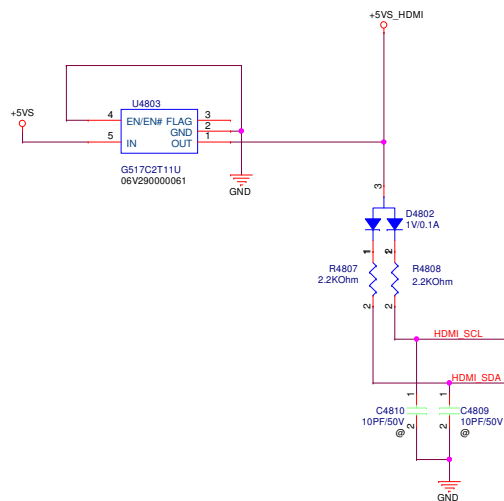
D-SUB Connector





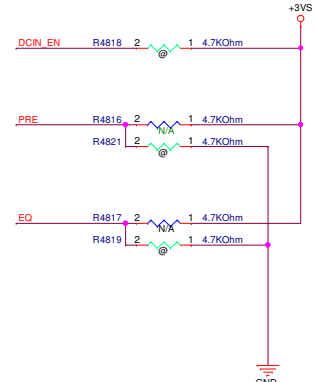
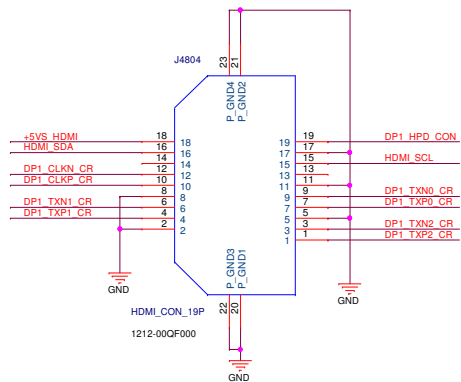
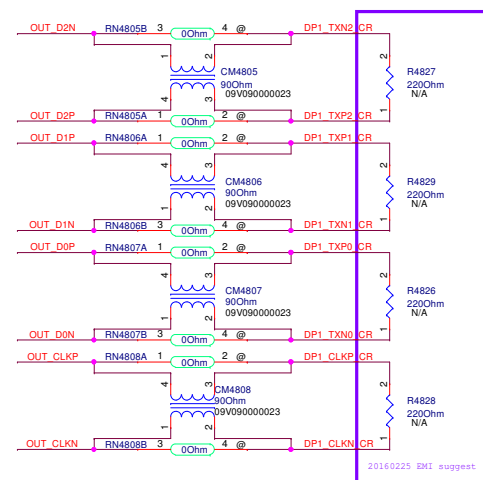
HDMI

Vinafix.com



DCIN_EN : DC coupling enable; Internal pull down at ~150k次, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input
PRE : Output pre-emphasis setting; Internal pull down at ~150k次, 3.3V I/O.
L: no pre-emphasis
H: 2.5dB pre-emphasis
EQ : Receiver equalization setting; Internal pull down at ~150k次, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
M: programmable EQ for channel loss up to 8.6dB @ 3Gbps

+12VS 28,31,57,62,91
+5VS 31,36,45,46,50,51,56,57,67,80,87,91
+3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,50,51,53,57,61,62,67,91,92
+1.5VS 36,57,85





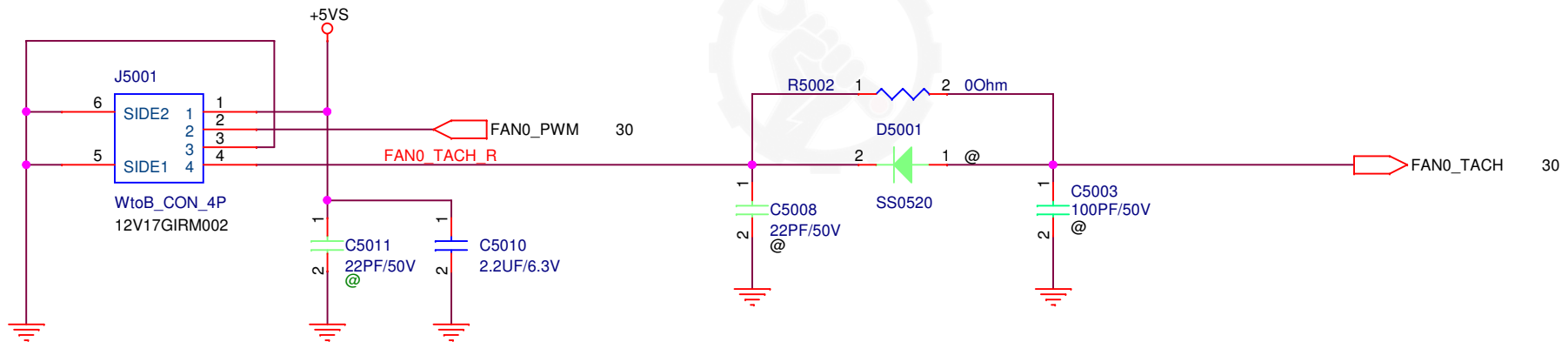
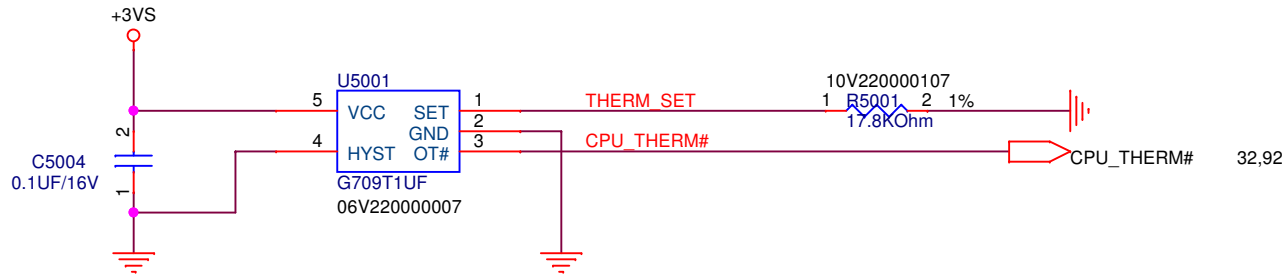
Vinafix.com



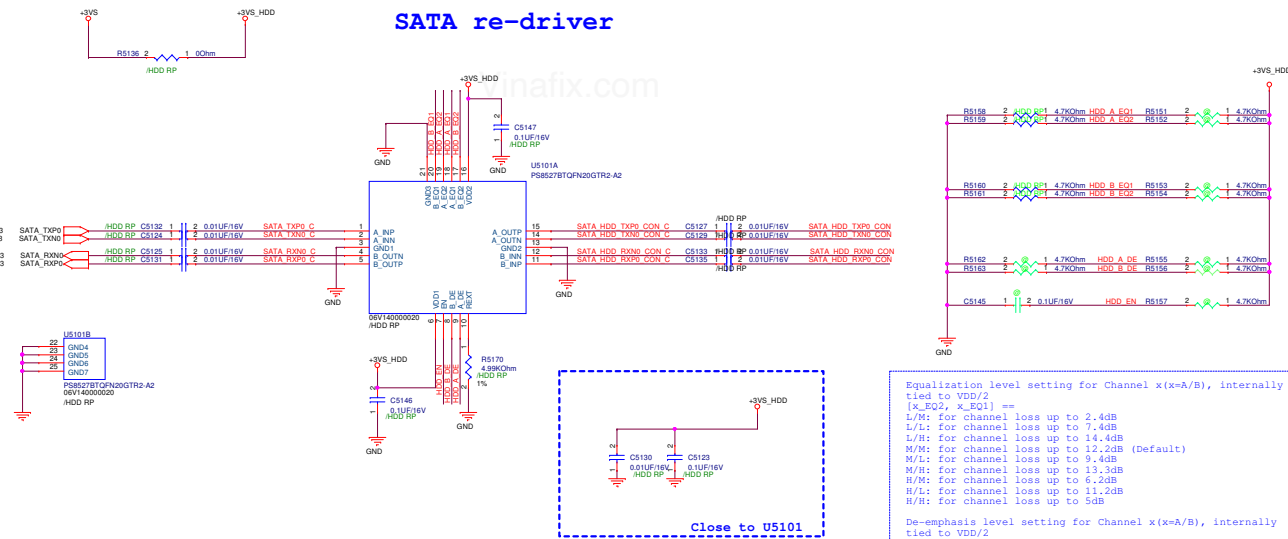
<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name KTRUG_25W	Rev 1.1	
Date: Tuesday, September 06, 2016		Sheet	49 of 108

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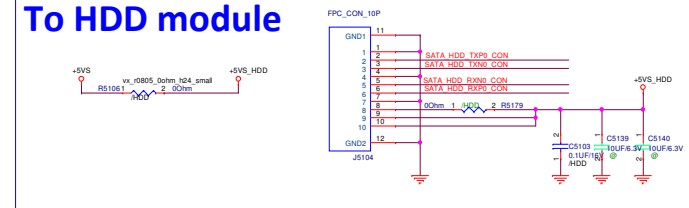
+3VS  +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,51,53,57,61,62,67,91,92
+5VS  +5VS 31,36,45,46,48,51,56,57,67,80,87,91



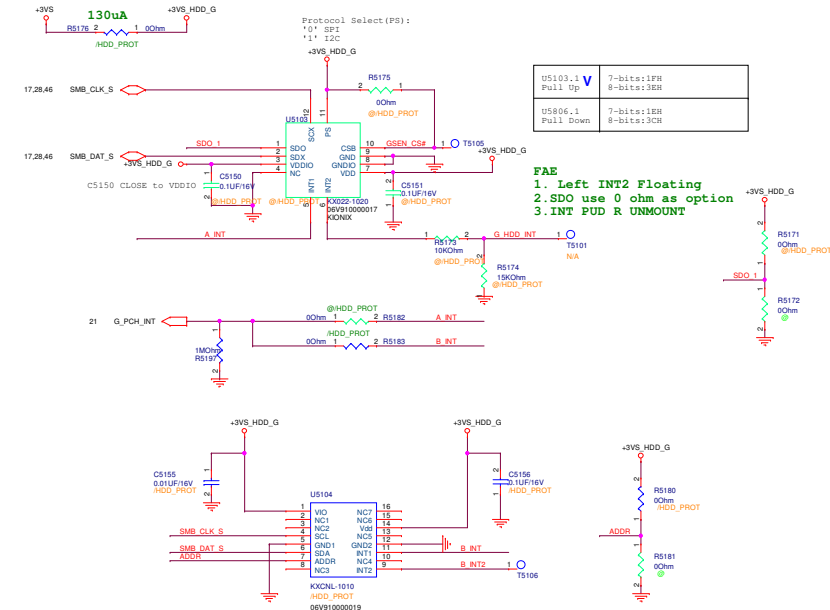
SATA re-driver



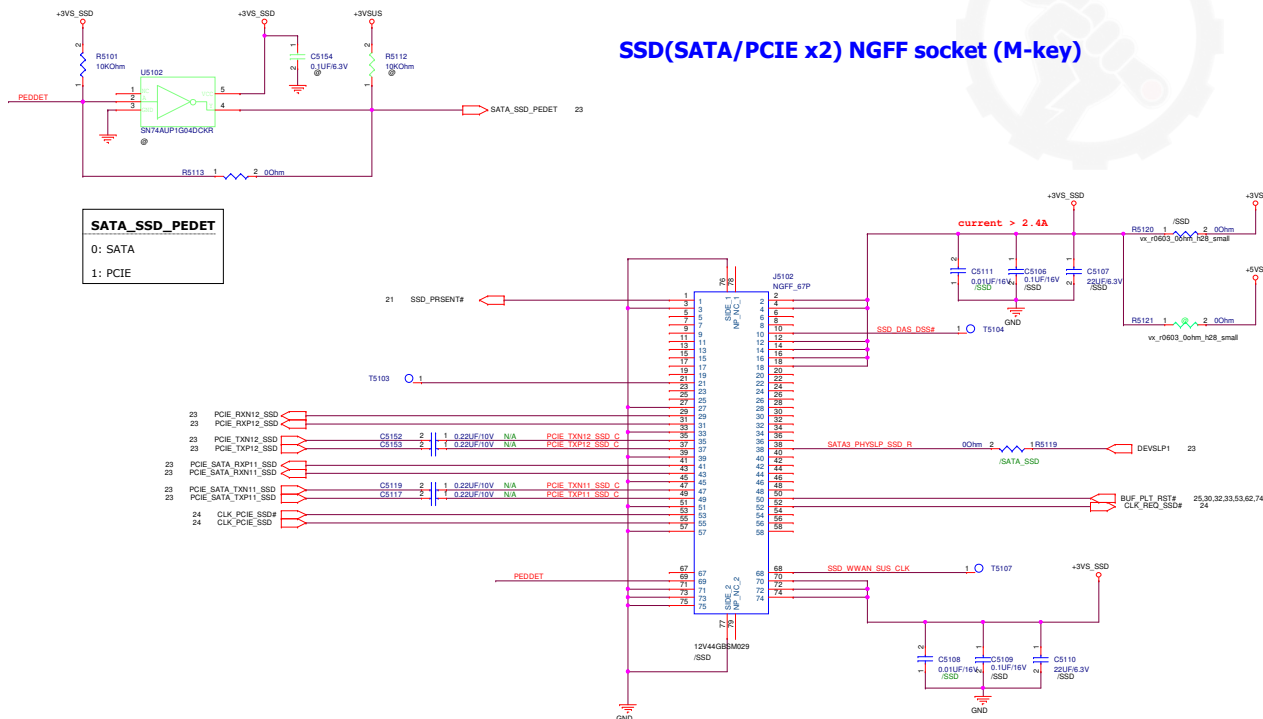
To HDD module



HDD G-Sensor



SSD(SATA/PCIE x2) NGFF socket (M-key)

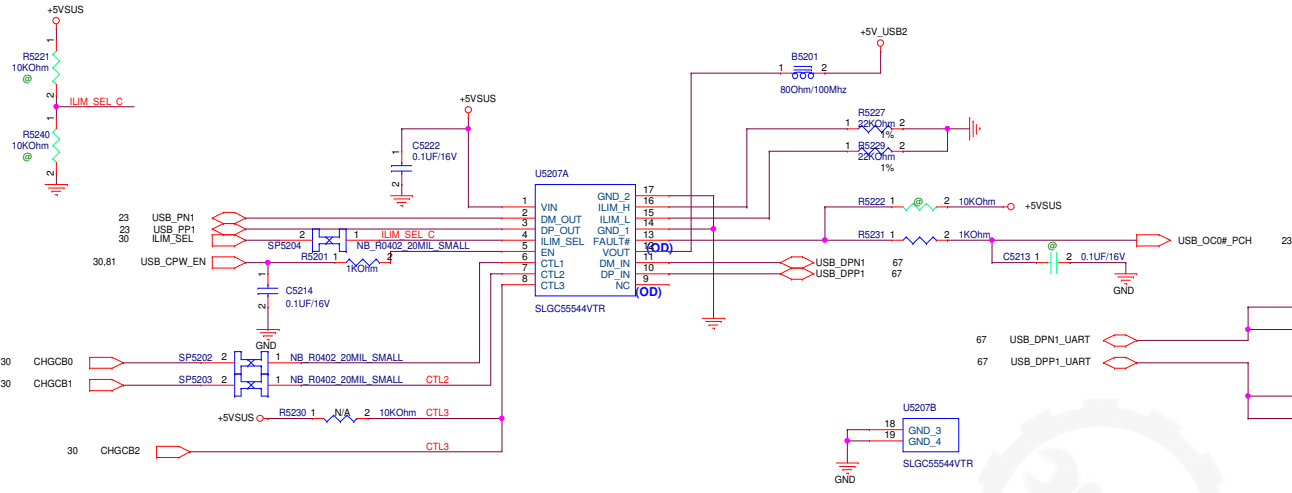


Variant Name:

USB 3.0 ports x 1 with Sleep & Charge Left_Down
TPS2544 Device True Table

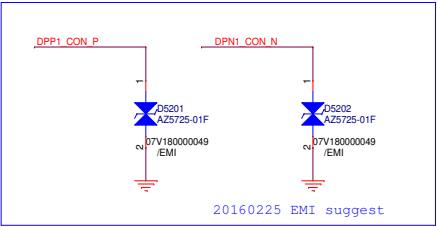
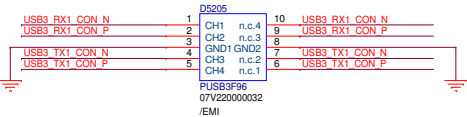
Vinafix.com

22k is to set current limit at 2.2A in DCP and CDP
47k is to set current limit at 1A in SDP

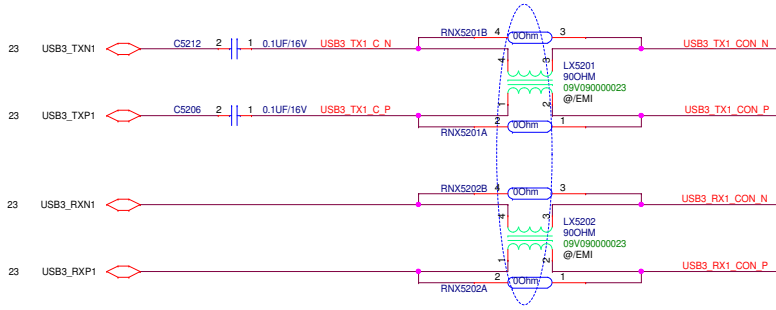


System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

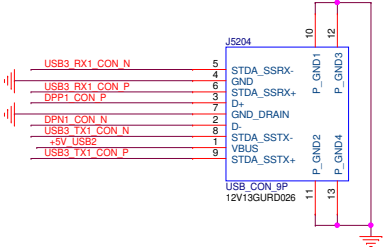
PLACE ESD Diodes near USB Connector



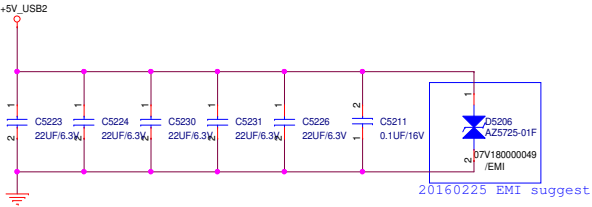
+5VSUS 41,42,56,67,81
+3VSUS 4,24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92



Colay



Colay

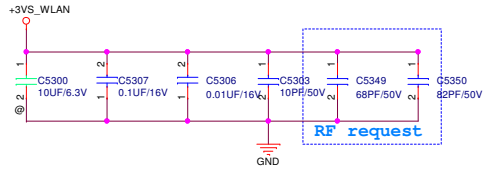


20160225 EMI suggest

WLAN/ WiGig / BT

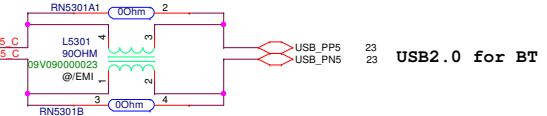
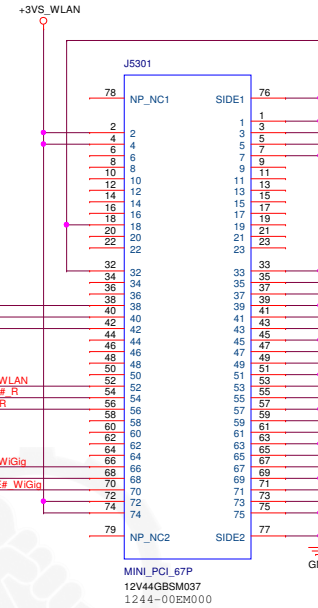
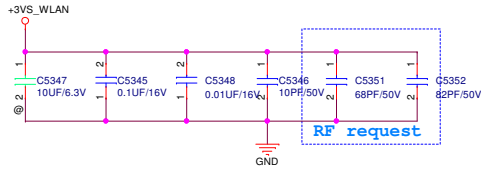
Place 0.1UF near pin 2,4

Place 10UF near +3V_WLAN_WP1 source side.

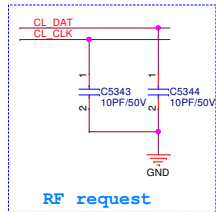
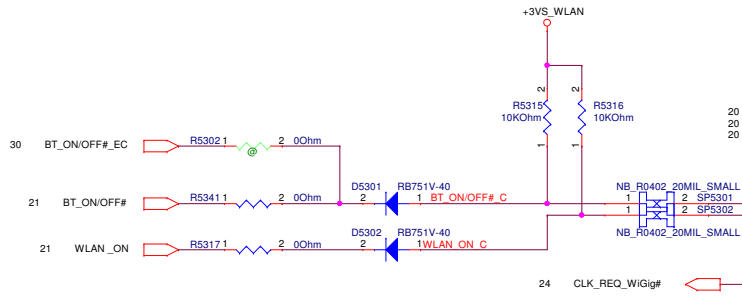


Place 0.1UF near pin 72,74.

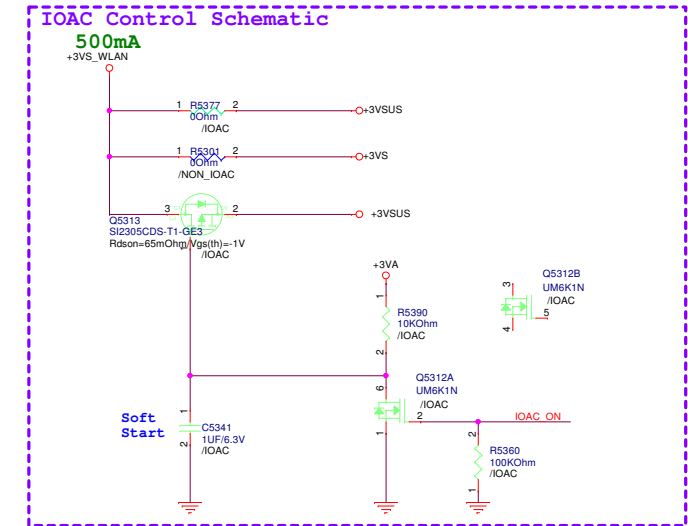
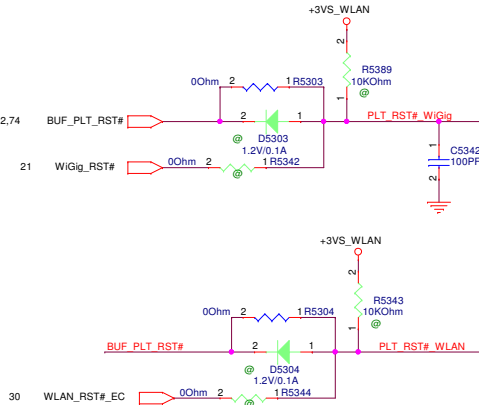
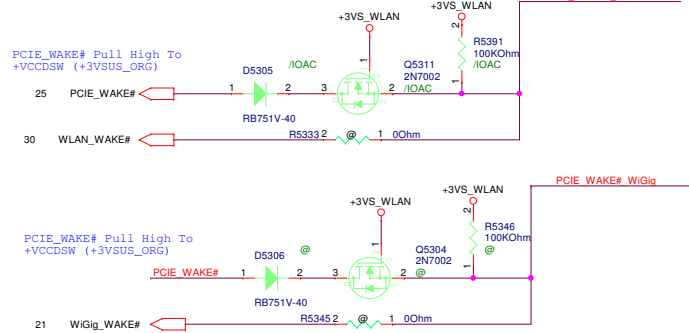
Place 10UF near +3V_WLAN_WP1 source side.



3 USB2.0 for BT



For USI W0096 Module Card



<Variant Name>

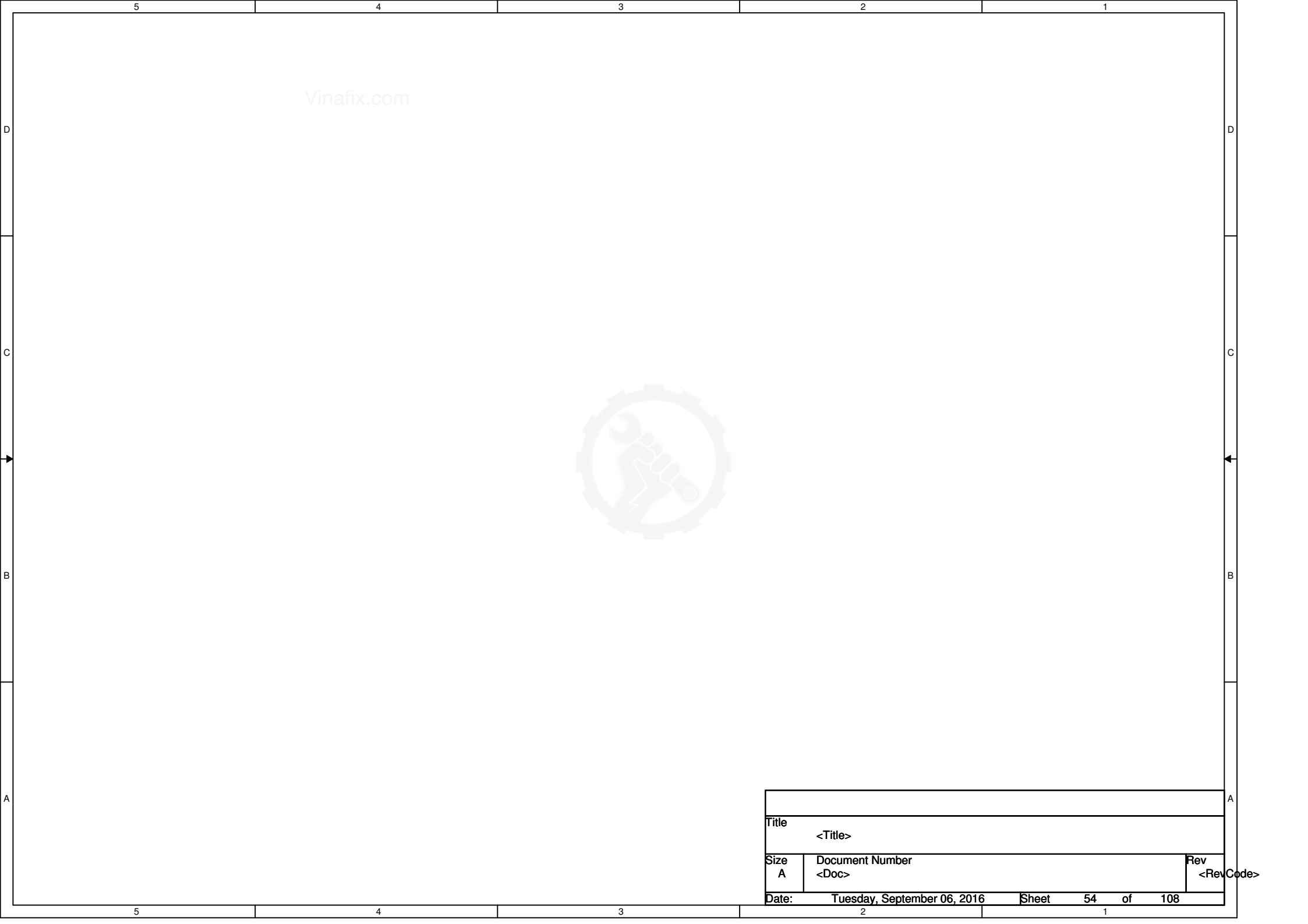
PEGATRON Title : WLAN/ WiGig / BT

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW4 Engineer: *Bill Yang*

Size	Project Name	Rev
Custom	P4	1.0

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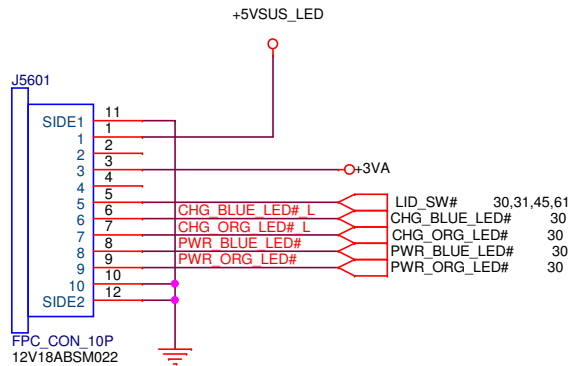
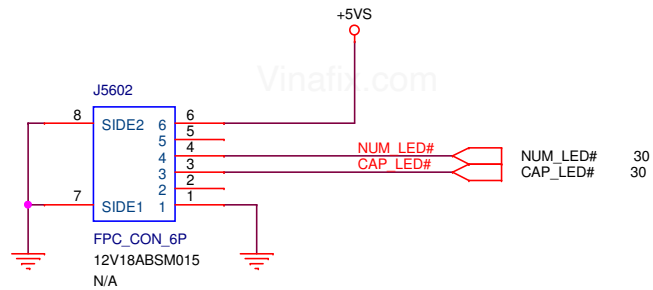


				A
Title				
<Title>				
Size	Document Number			Rev
A	<Doc>			<RevCode>
Date:	Tuesday, September 06, 2016		Sheet	54 of 108

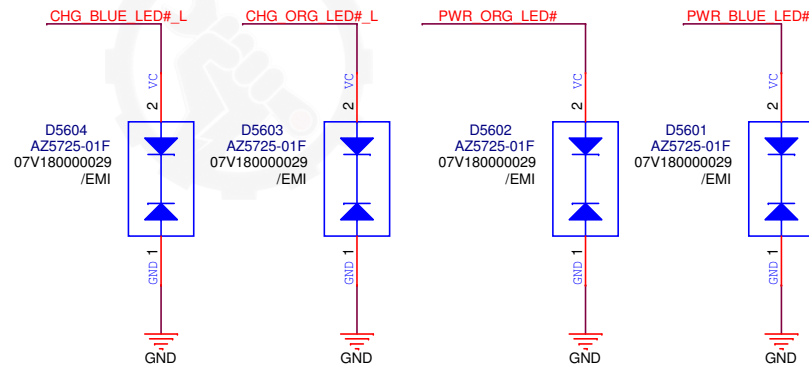
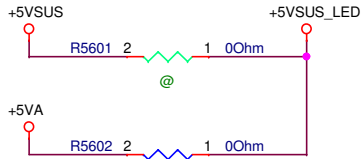
Vinafix.com

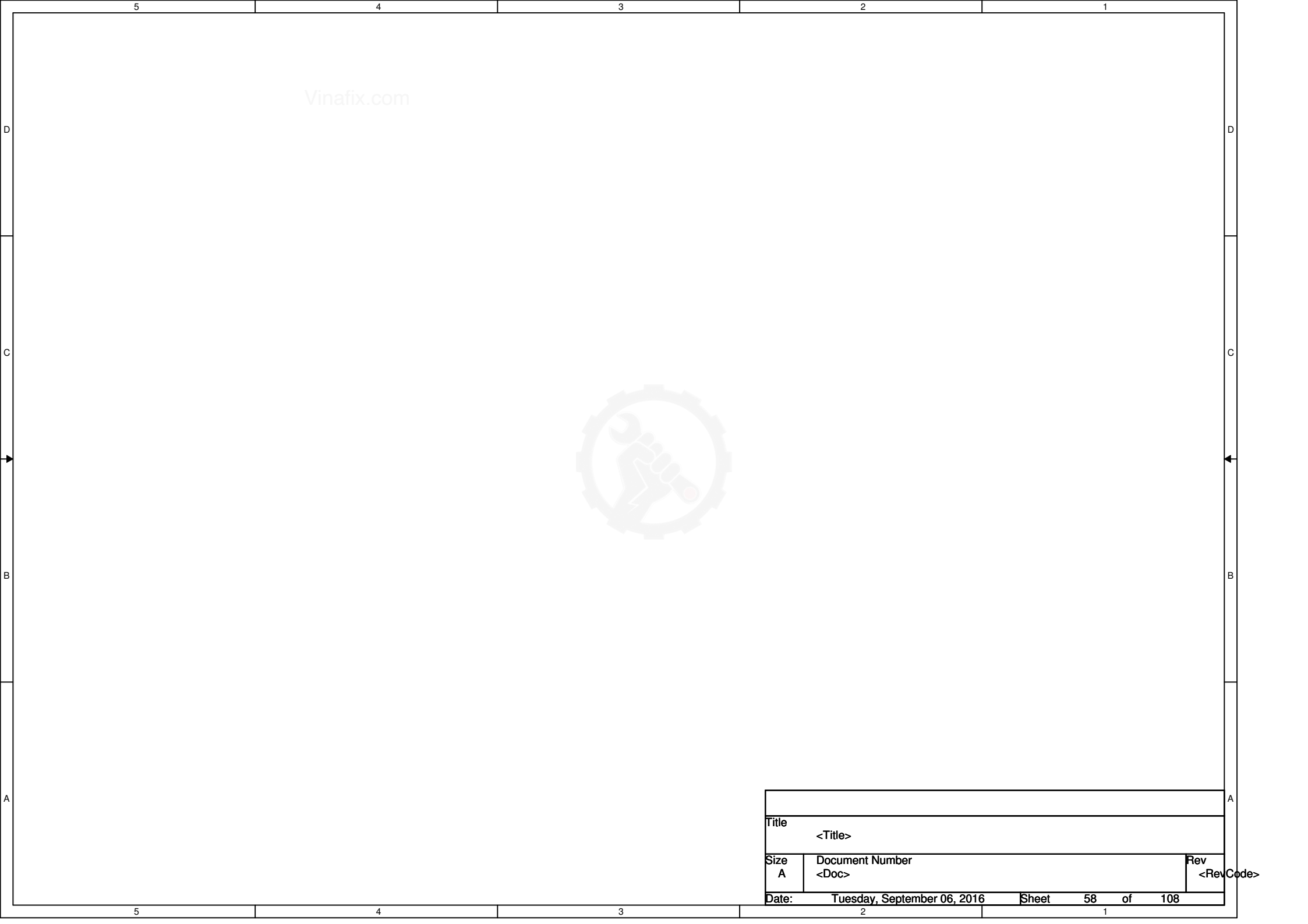


Title				<Title>	
Size	Document Number			Rev	
A	KTKUG_25W			1.1	
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+5VS 31,36,45,46,48,50,51,57,67,80,87,91
+5VSUS 41,42,52,67,81
+3VA 24,30,31,36,41,43,53,57,67,81,88,93





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				A
Title				
<Title>				
Size	Document Number			Rev
A	<Doc>			<RevCode>
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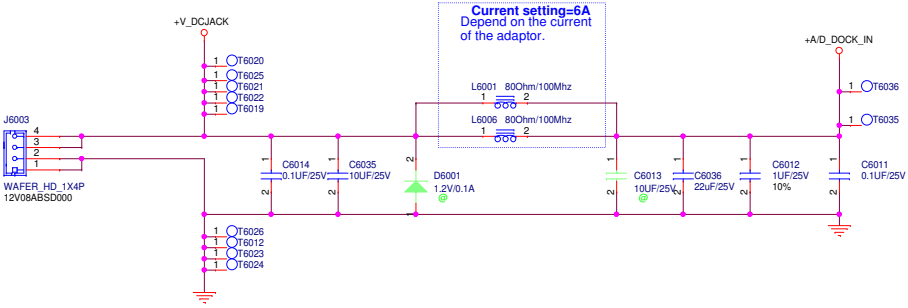
Vinafix.com



<Variant Name>			
PEGATRON		Title :	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size C	Project Name KTRUG_25W	Rev 1.1	
Date: Tuesday, September 06, 2016		Sheet 59 of 108	

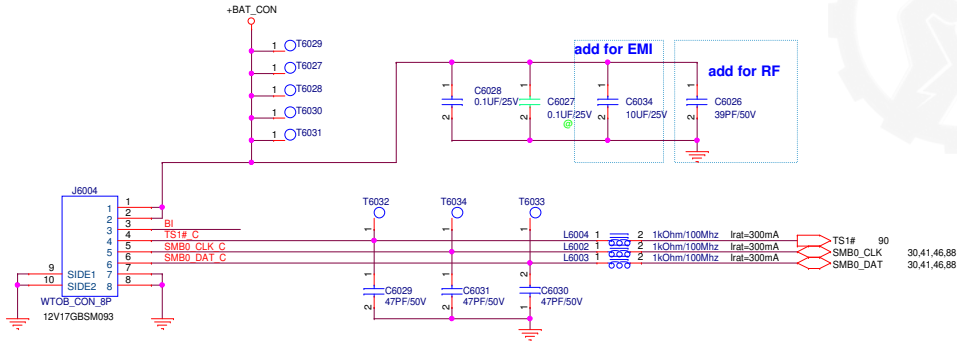
Vinafix.com

DC Jack WTB CONN

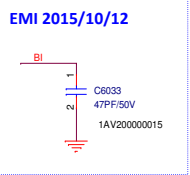
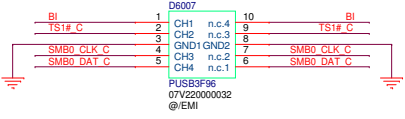
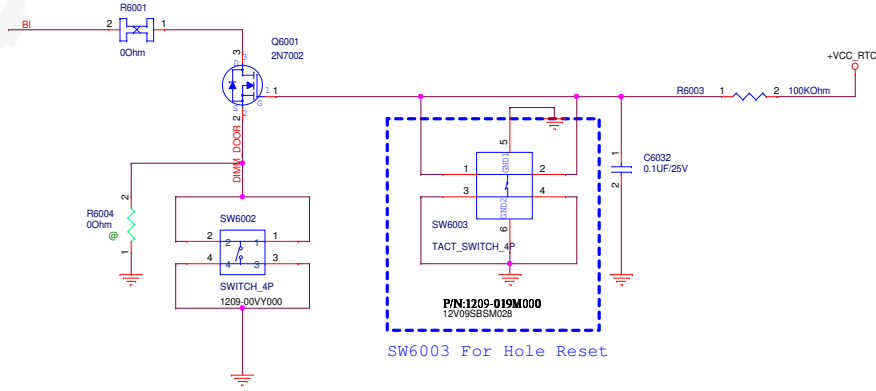


+VCC_RTC	+VCC_RTC	24,25,26,36
+3VA_EC	+3VA_EC	28,30,32
+3VA_O	+3VA	24,30,31,36,41,43,53,56,57,67,81,88,93
+5VA_O	+5VA	31,56,81
+1.0VSUS	+1.0VSUS	26,82
+1.8VSUS	+1.8VSUS	9,21,24,26,84
+3VSUS	+3VSUS	4,24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+5VSUS	+5VSUS	41,42,52,56,67,81
+12VSUS	+12VSUS	81,91
+3V	+3V	25,31,44,57,67,82,91
+12V	+12V	91
+3VS	+3VS	3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+5VS	+5VS	31,36,45,46,48,50,51,56,57,67,80,87,91
+12VS	+12VS	28,31,57,62,91
+AC_BAT_SYS	+AC_BAT_SYS	43,45,80,81,82,83,85,87,88
+A/D_DOCK_IN	+A/D_DOCK_IN	89
+BAT_CON	+BAT_CON	88
+VCORE	+VCORE	5,57,80
+VCCGT	+VCCGT	6,57,80
+VCCSA	+VCCSA	7,57,80
+VCCIO	+VCCIO	3,7,57,91
+RTCBAT	+RTCBAT	24

Battery Connector

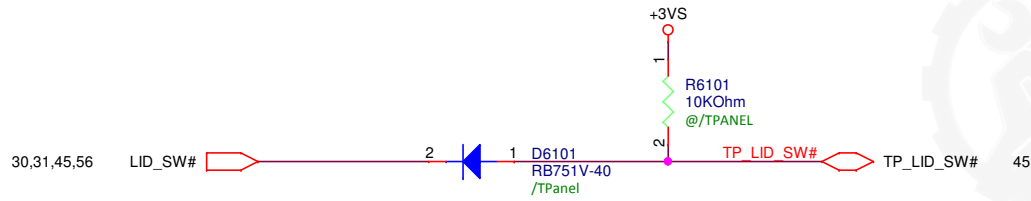


客戶設計的原因是因為若有100ohm可能會造成分壓而導致pin無法拉到low, 故改為0ohm



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+5VS 31,36,45,46,48,50,51,56,57,67,80,87,91
+3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,62,67,91,92

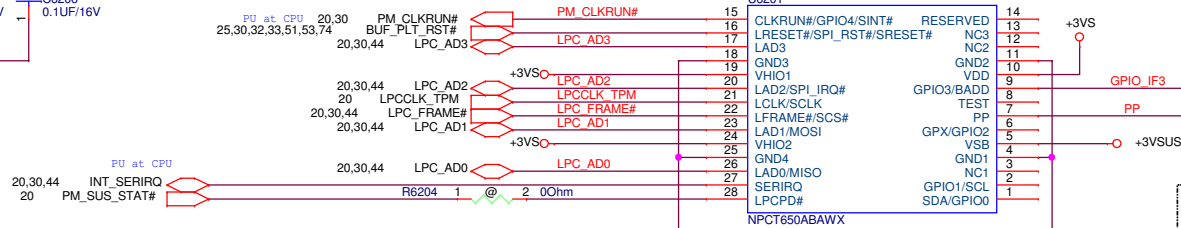
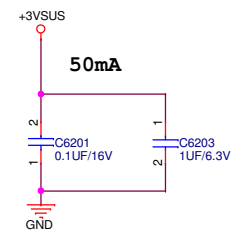
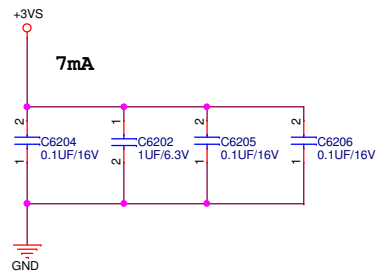


<Variant Name>

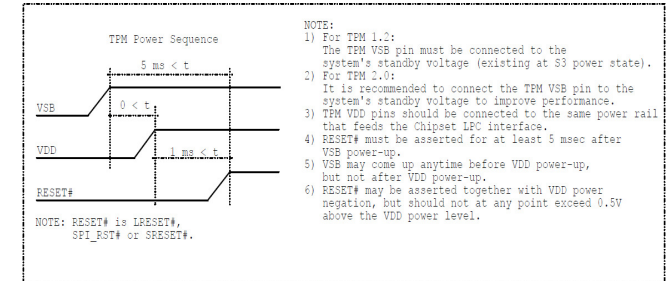
PEGATRON		Title : Touch Panel Conn	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Bill Yang	
Size Custom	Project Name P4		Rev 1.0
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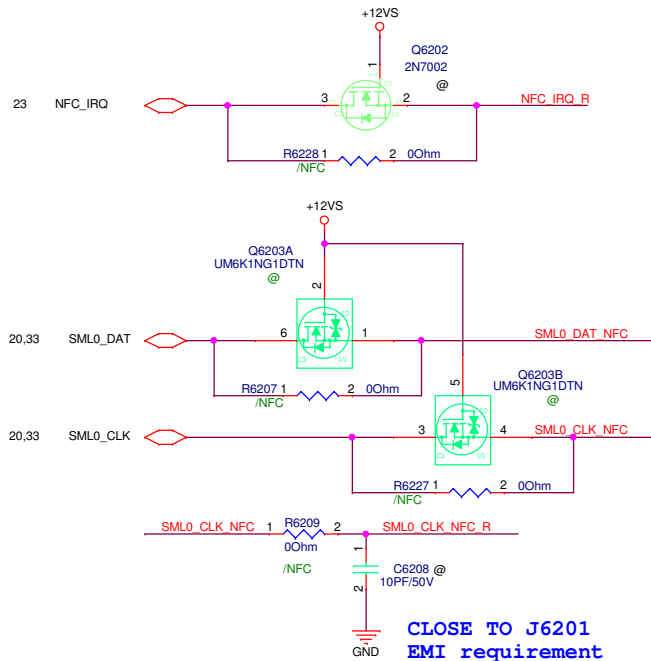
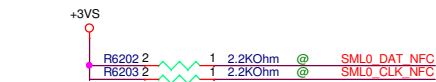
TPM



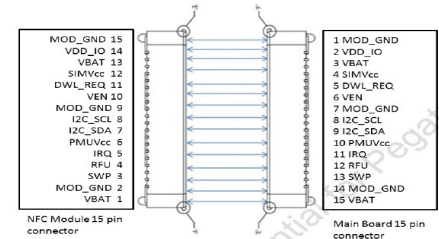
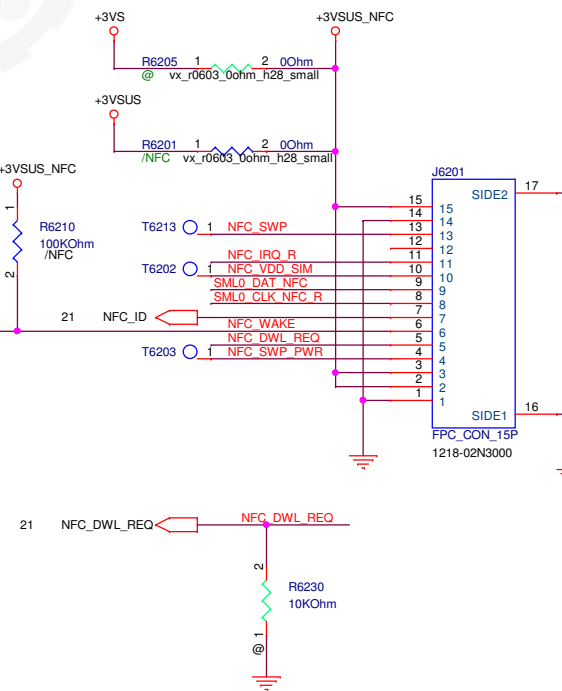
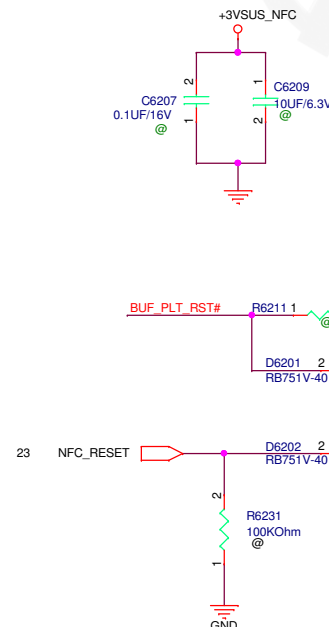
Slave address is for I2C interface, and is selected by BADD




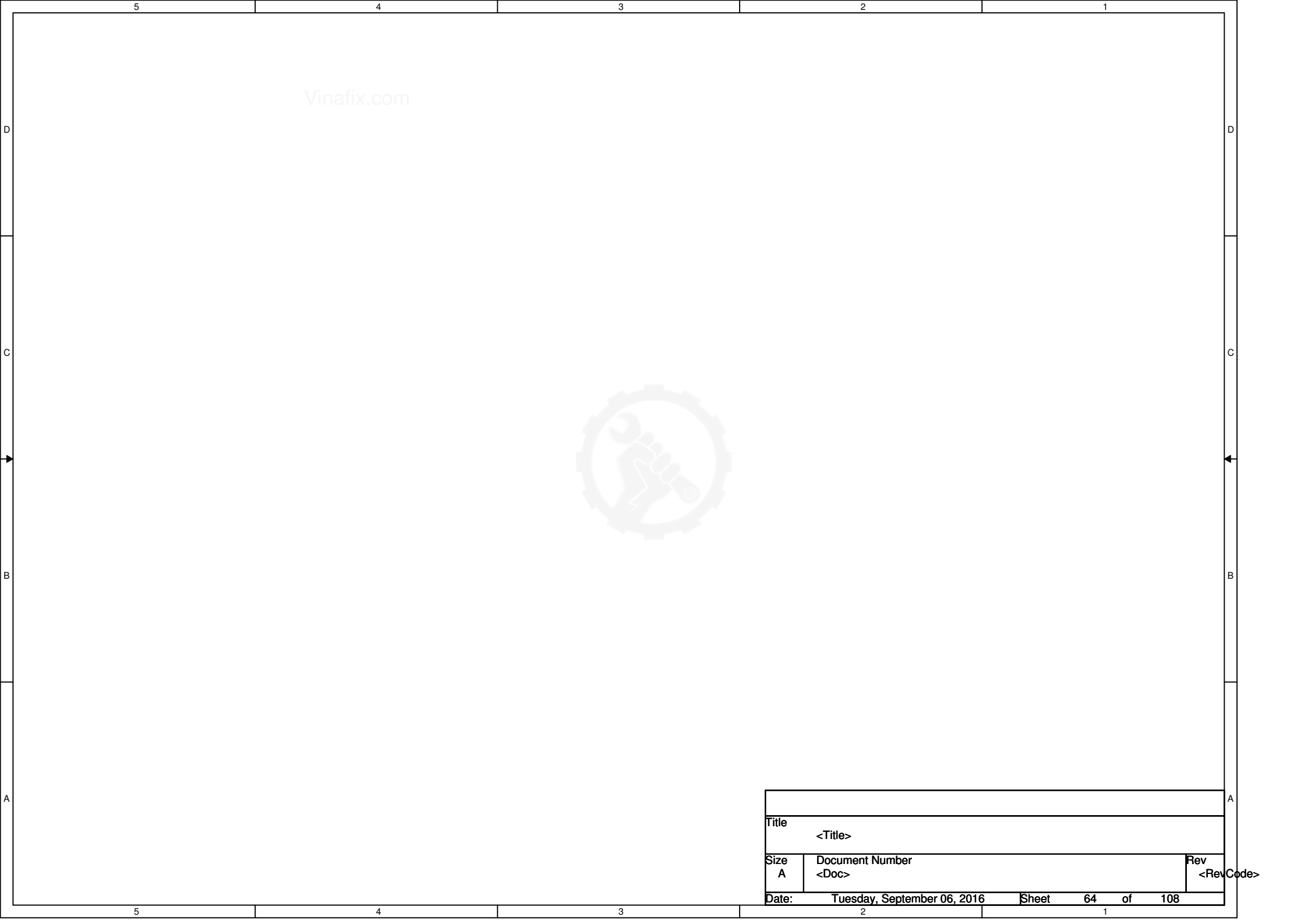
NFC



CLOSE TO J6201
EMI requirement



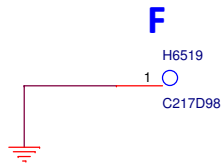
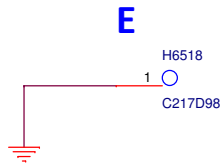
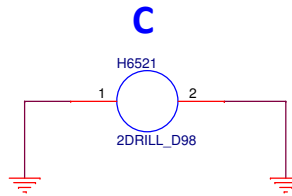
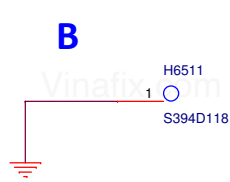
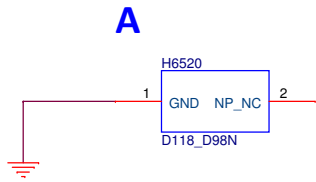
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D	Vinafix.com					D																				
C						C																				
B						B																				
A	<table><tr><td colspan="5"></td></tr><tr><td colspan="5">Title <Title></td></tr><tr><td>Size A</td><td colspan="3">Document Number KTKUG_25W</td><td>Rev 1.1</td></tr><tr><td colspan="5">Date: Tuesday, September 06, 2016 Sheet 63 of 108</td></tr></table>										Title <Title>					Size A	Document Number KTKUG_25W			Rev 1.1	Date: Tuesday, September 06, 2016 Sheet 63 of 108					A
Title <Title>																										
Size A	Document Number KTKUG_25W			Rev 1.1																						
Date: Tuesday, September 06, 2016 Sheet 63 of 108																										
	5	4	3	2	1																					



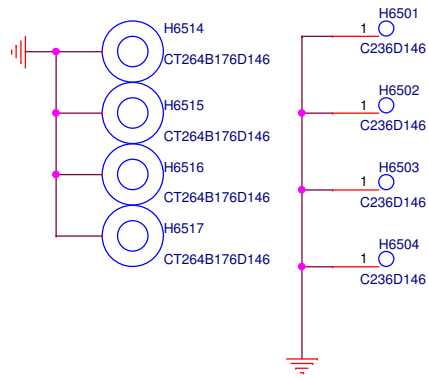
Vinafix.com



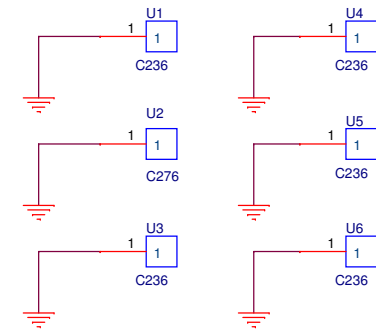
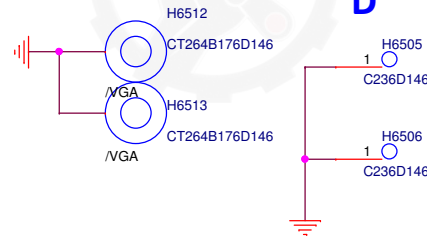
Title <Title>			
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BGA
CPU NUTx4

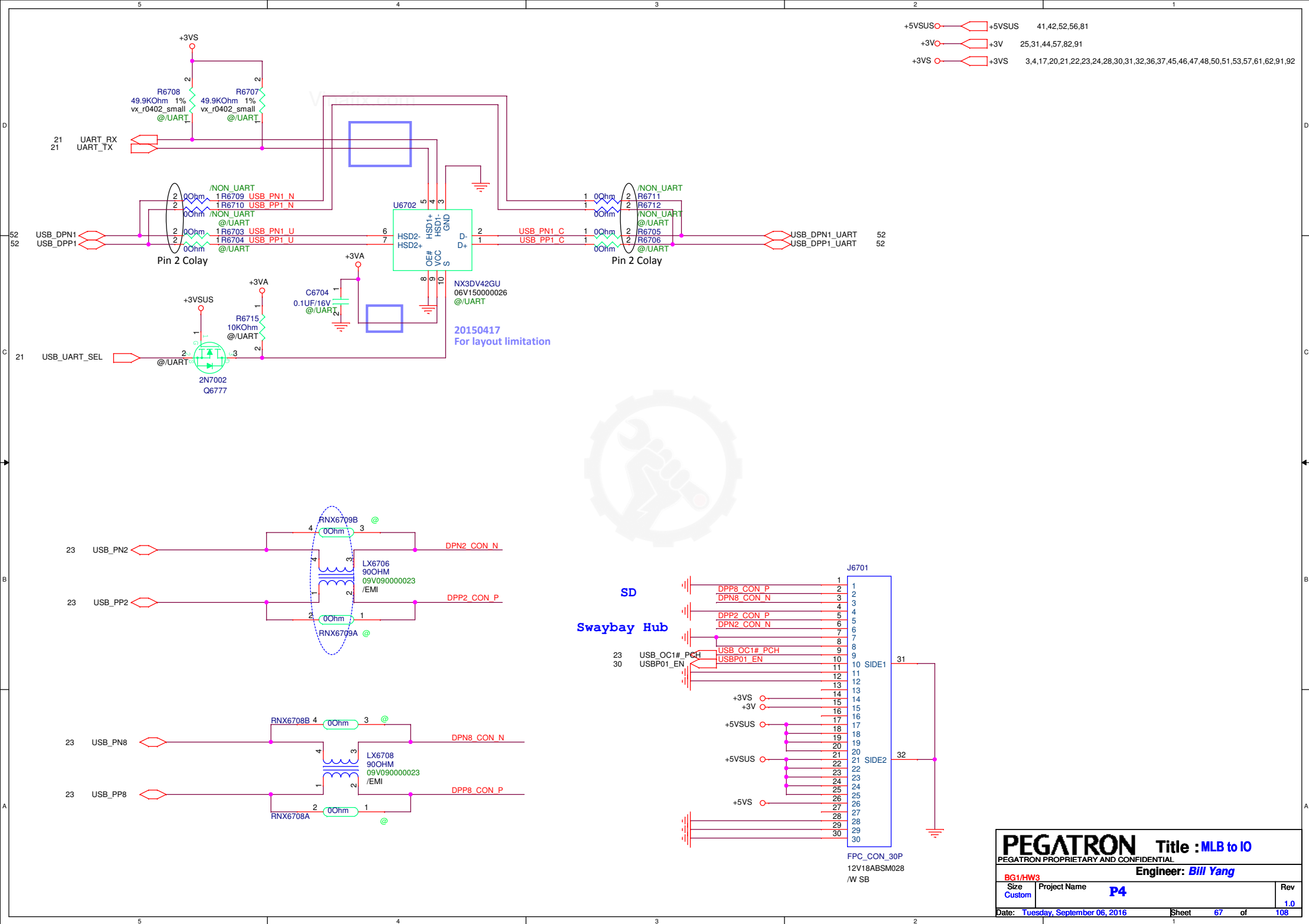


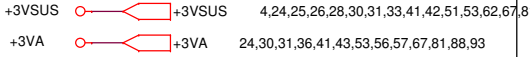
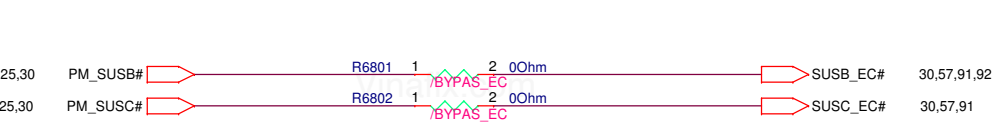
BGA
GPU NUTx2



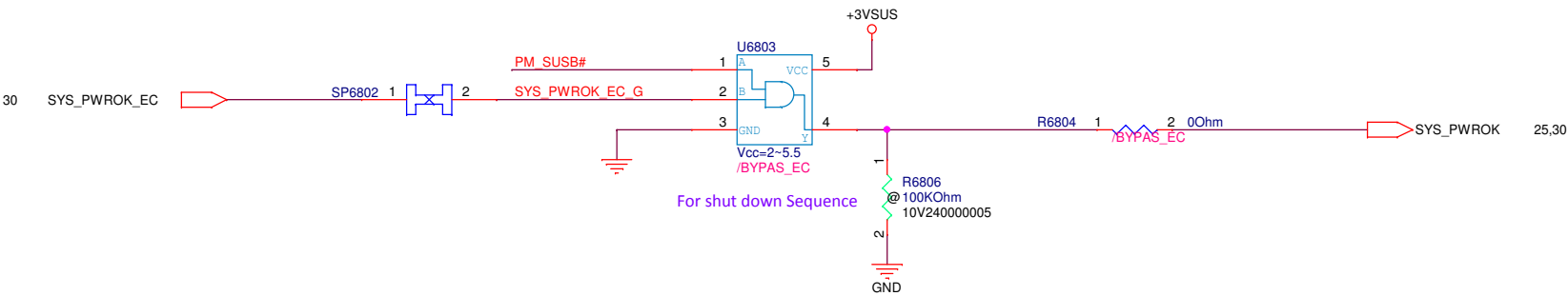
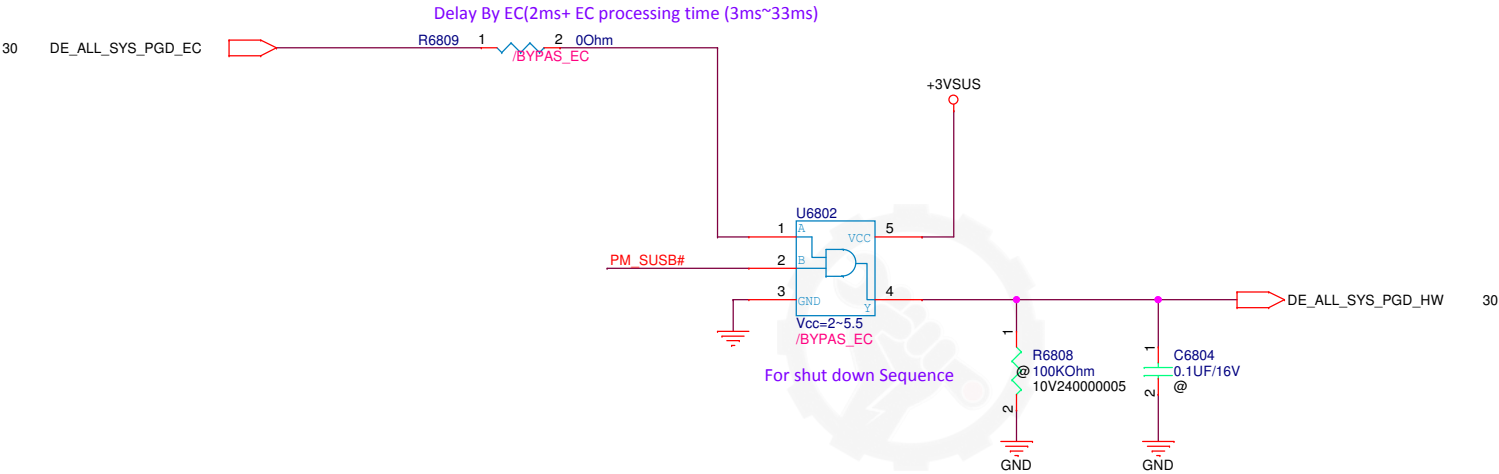
<Variant Name>

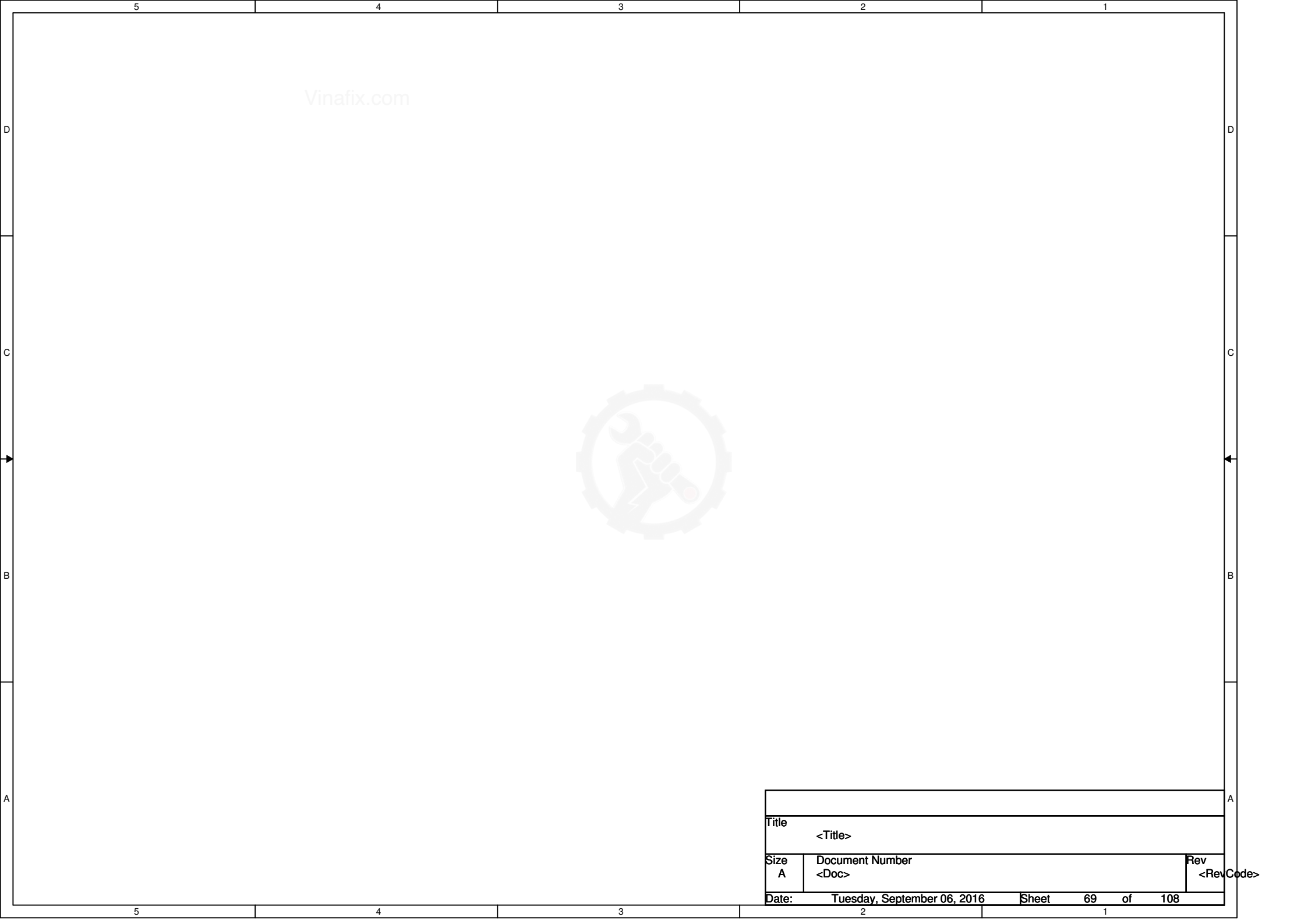
PEGATRON		Title: ME_CONN,Skew Hole	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Bill Yang	
Size Custom	Project Name P4		Rev 1.0
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For Intel power sequence request
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

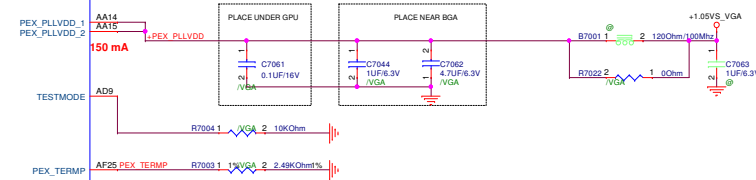
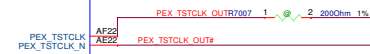
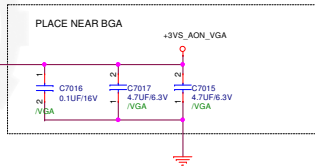
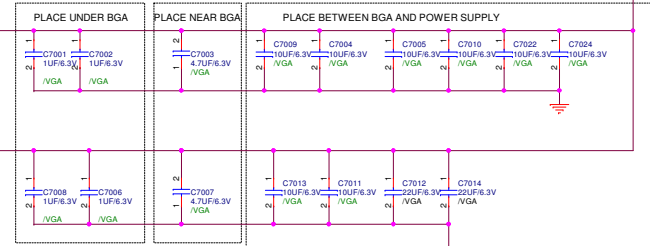
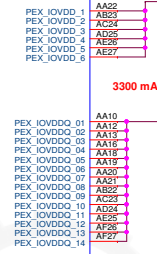
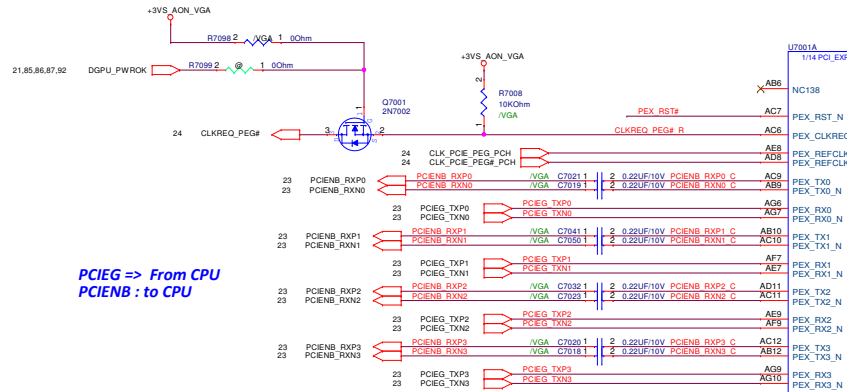
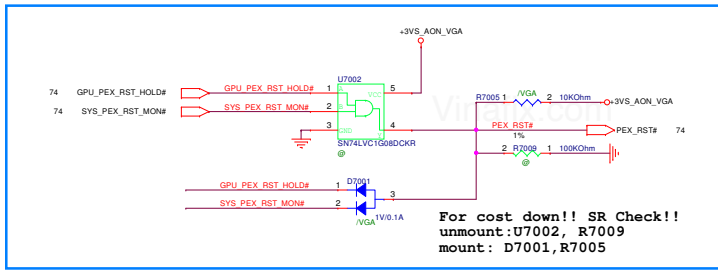




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Title <Title>			
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N16S-GTR-S-A2
02V0A0000038

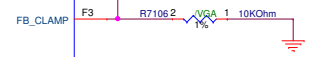
76 FBAD[0..63]
76 FBA_CMD[0..31]
76 FBA_DB[0..7]
76 FBA_EDC[0..7]

U7001B
2/14 FBA
FBAD0 E18 FBA D0
FBAD1 F18 FBA D1
FBAD2 E16 FBA D2
FBAD3 F17 FBA D3
FBAD4 D20 FBA D4
FBAD5 D21 FBA D5
FBAD6 F20 FBA D6
FBAD7 E21 FBA D7
FBAD8 E15 FBA D8
FBAD9 D15 FBA D9
FBAD10 F15 FBA D10
FBAD11 F13 FBA D11
FBAD12 C13 FBA D12
FBAD13 B13 FBA D13
FBAD14 E13 FBA D14
FBAD15 D13 FBA D15
FBAD16 B15 FBA D16
FBAD17 C16 FBA D17
FBAD18 A13 FBA D18
FBAD19 A15 FBA D19
FBAD20 B18 FBA D20
FBAD21 A18 FBA D21
FBAD22 A19 FBA D22
FBAD23 C19 FBA D23
FBAD24 B24 FBA D24
FBAD25 C23 FBA D25
FBAD26 A25 FBA D26
FBAD27 A24 FBA D27
FBAD28 A21 FBA D28
FBAD29 B21 FBA D29
FBAD30 C20 FBA D30
FBAD31 C21 FBA D31
FBAD32 R22 FBA D32
FBAD33 R24 FBA D33
FBAD34 T22 FBA D34
FBAD35 R23 FBA D35
FBAD36 N25 FBA D36
FBAD37 N26 FBA D37
FBAD38 N23 FBA D38
FBAD39 N24 FBA D39
FBAD40 V23 FBA D40
FBAD41 V22 FBA D41
FBAD42 T23 FBA D42
FBAD43 U22 FBA D43
FBAD44 Y24 FBA D44
FBAD45 AA24 FBA D45
FBAD46 Y22 FBA D46
FBAD47 AA23 FBA D47
FBAD48 AB27 FBA D48
FBAD49 AB25 FBA D49
FBAD50 AD26 FBA D50
FBAD51 AC25 FBA D51
FBAD52 AA27 FBA D52
FBAD53 AA26 FBA D53
FBAD54 W26 FBA D54
FBAD55 Y25 FBA D55
FBAD56 R26 FBA D56
FBAD57 T25 FBA D57
FBAD58 N27 FBA D58
FBAD59 R27 FBA D59
FBAD60 V26 FBA D60
FBAD61 V27 FBA D61
FBAD62 W27 FBA D62
FBAD63 W25 FBA D63

FBA_DB0 D19 FBA_D0M0
FBA_DB1 D14 FBA_D0M1
FBA_DB2 C17 FBA_D0M2
FBA_DB3 C22 FBA_D0M3
FBA_DB4 P24 FBA_D0M4
FBA_DB5 W24 FBA_D0M5
FBA_DB6 AA25 FBA_D0M6
FBA_DB7 U25 FBA_D0M7

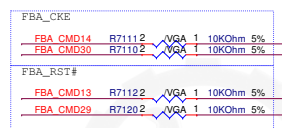
FBA_EDC0 E19 FBA_DQS_WP0
FBA_EDC1 C15 FBA_DQS_WP1
FBA_EDC2 B16 FBA_DQS_WP2
FBA_EDC3 B22 FBA_DQS_WP3
FBA_EDC4 R25 FBA_DQS_WP4
FBA_EDC5 W23 FBA_DQS_WP5
FBA_EDC6 AB26 FBA_DQS_WP6
FBA_EDC7 T26 FBA_DQS_WP7

Vinafix co GPU_FB_CLAMP_R R7107 2 1 0Ohm GC6_FB_EN 21,74,85



+1.35VS_VGA
+1.05VS_VGA

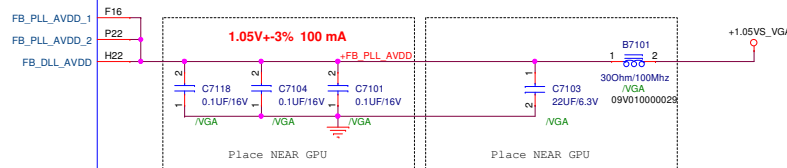
FBA_CMD0 C27 FBA_CMD0
FBA_CMD1 C26 FBA_CMD1
FBA_CMD2 F24 FBA_CMD2
FBA_CMD3 F23 FBA_CMD3
FBA_CMD4 D27 FBA_CMD4
FBA_CMD5 D26 FBA_CMD5
FBA_CMD6 F25 FBA_CMD6
FBA_CMD7 F26 FBA_CMD7
FBA_CMD8 F23 FBA_CMD8
FBA_CMD9 G22 FBA_CMD9
FBA_CMD10 G23 FBA_CMD10
FBA_CMD11 G24 FBA_CMD11
FBA_CMD12 F27 FBA_CMD12
FBA_CMD13 G25 FBA_CMD13
FBA_CMD14 G27 FBA_CMD14
FBA_CMD15 G26 FBA_CMD15
FBA_CMD16 M24 FBA_CMD16
FBA_CMD17 M23 FBA_CMD17
FBA_CMD18 K24 FBA_CMD18
FBA_CMD19 K23 FBA_CMD19
FBA_CMD20 M27 FBA_CMD20
FBA_CMD21 M25 FBA_CMD21
FBA_CMD22 M25 FBA_CMD22
FBA_CMD23 K26 FBA_CMD23
FBA_CMD24 K22 FBA_CMD24
FBA_CMD25 J23 FBA_CMD25
FBA_CMD26 J25 FBA_CMD26
FBA_CMD27 J24 FBA_CMD27
FBA_CMD28 K27 FBA_CMD28
FBA_CMD29 K25 FBA_CMD29
FBA_CMD30 J27 FBA_CMD30
FBA_CMD31 J26 FBA_CMD31



FBA_CMD32 B19
FBA_CMD34 F22 R7101 1 2 60.4Ohm 1%
FBA_CMD35 J22 R7102 1 2 60.4Ohm 1%

FBA_CLK0 D24 FBA_CLK0 76
FBA_CLK0_N D25 FBA_CLK0# 76
FBA_CLK1 M22 FBA_CLK1 76
FBA_CLK1_N M22 FBA_CLK1# 76

FBA_WCK01 D18 FBA_WCK01 76
FBA_WCK01_N C18 FBA_WCK01# 76
FBA_WCK23 D17 FBA_WCK23 76
FBA_WCK23_N D16 FBA_WCK23# 76
FBA_WCK45 T24 FBA_WCK45 76
FBA_WCK45_N U24 FBA_WCK45# 76
FBA_WCK67 V24 FBA_WCK67 76
FBA_WCK67_N V25 FBA_WCK67# 76



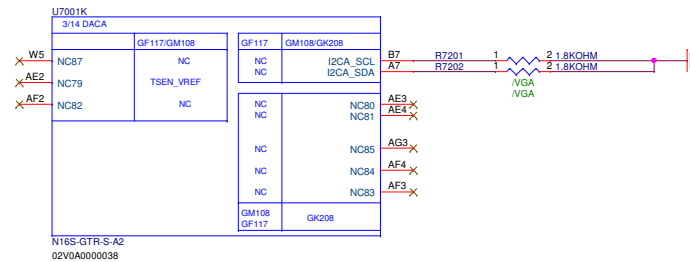
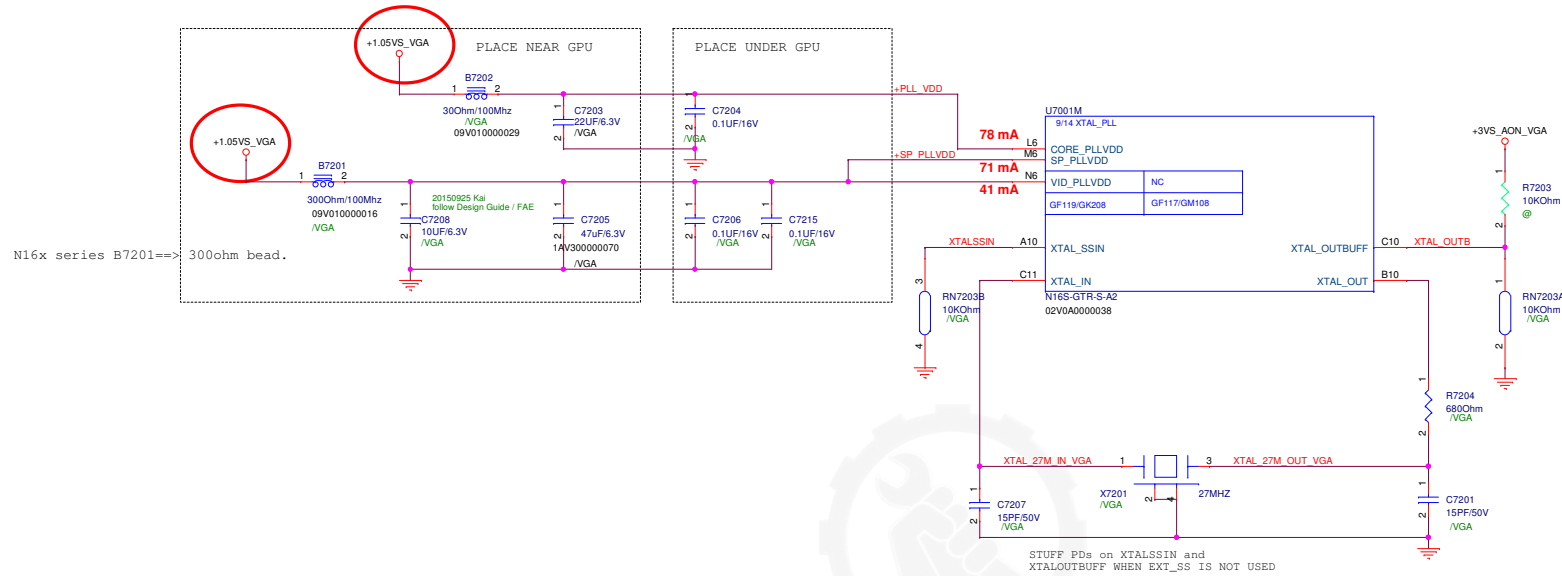
T7101
/VGA 1 FB_VREF D23
N16S-GTR-S-A2
02V0A000038

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+3VS_AON_VGA → +3VS_AON_VGA 57,70,74,75,91

+1.05VS_VGA → +1.05VS_VGA 57,70,71,86

20141024 Chris



PEGATRON Title : GPU(1)

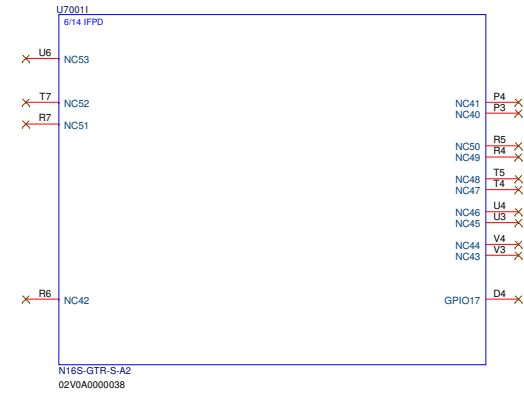
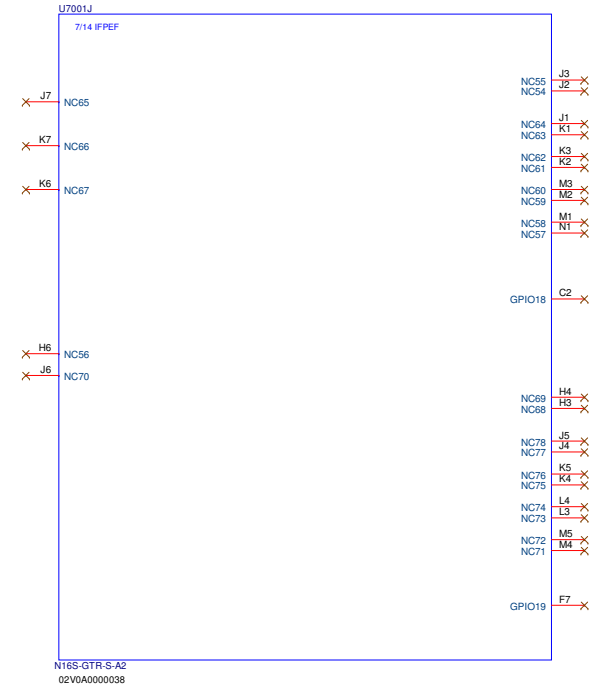
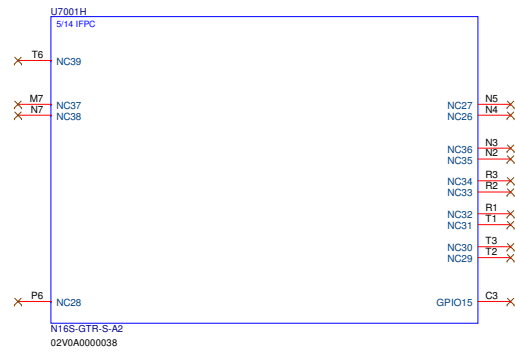
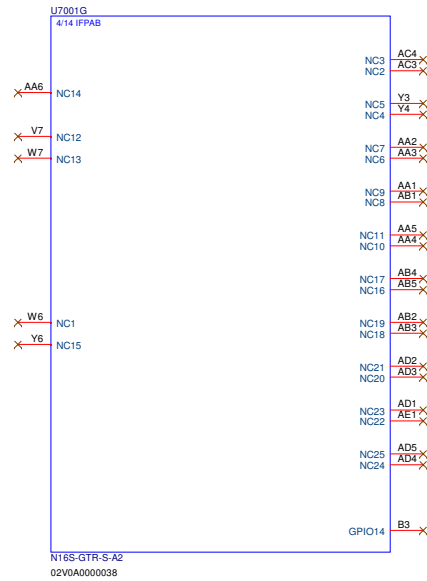
PEGATRON PROPRIETARY AND CONFIDENTIAL
Rev 1.0

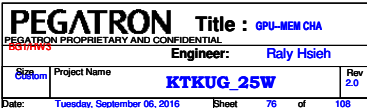
Size Custom Project Name **P4** Rev 1.0

Date: Tuesday, September 06, 2016 Sheet 72 of 108

Engineer: Bill Yang

LVDS





5

4

3

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D

C

C |

B

B

A

A

				A
Title <div style="border: 1px solid black; padding: 2px; text-align: center;"><Title></div>				
Size A	Document Number <div style="border: 1px solid black; padding: 2px; text-align: center;"><Doc></div>		Rev <div style="border: 1px solid black; padding: 2px; text-align: center;"><RevCode></div>	
Date: Tuesday, September 06, 2016 Sheet 77 of 108				

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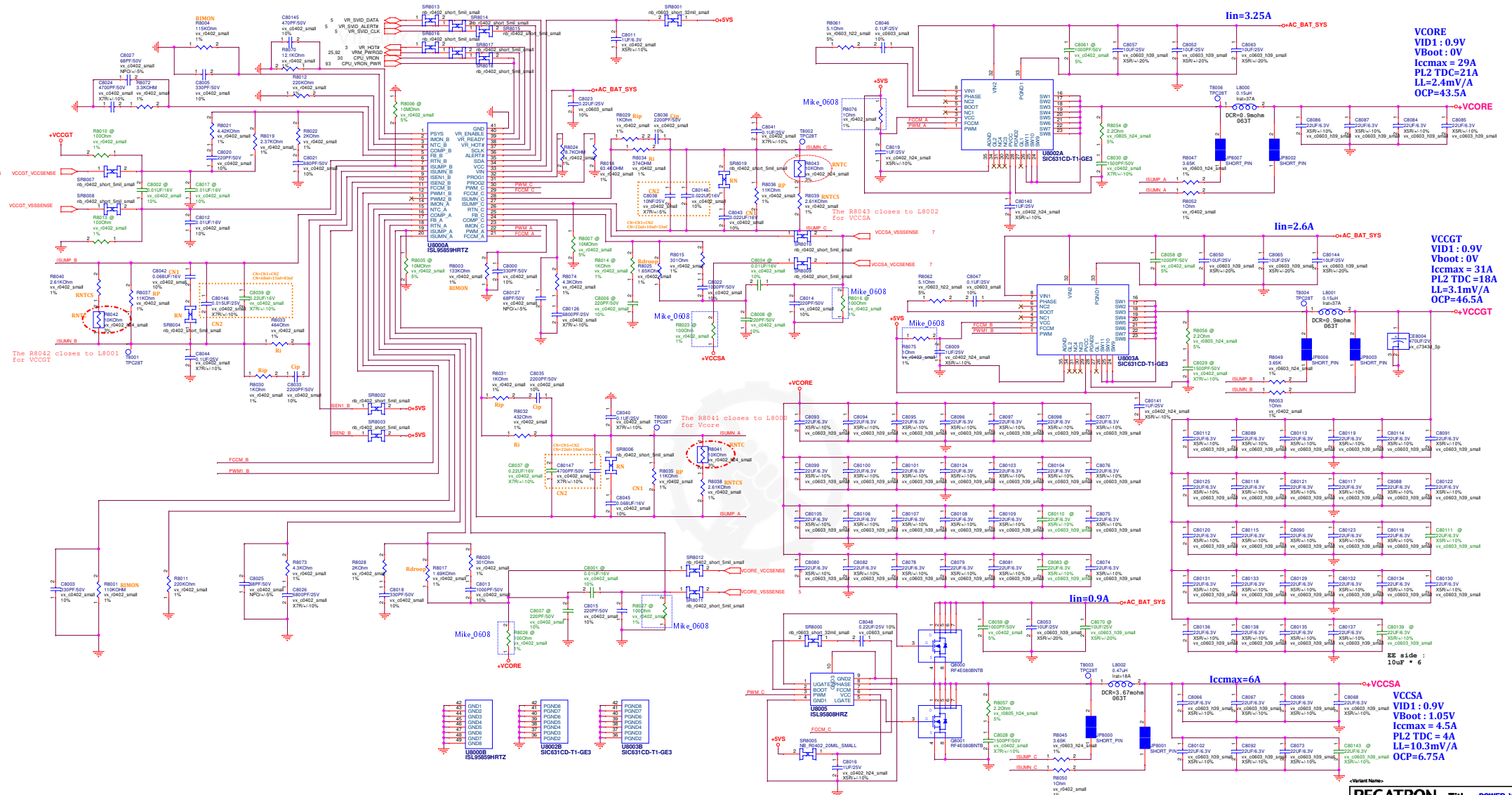
PEGATRON Title : ****		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: Raly Hsieh
Size A	Project Name KTKUG_25W	Rev 1.0
Date: Tuesday, September 06, 2016		Sheet 78 of 99

Vinafix.com



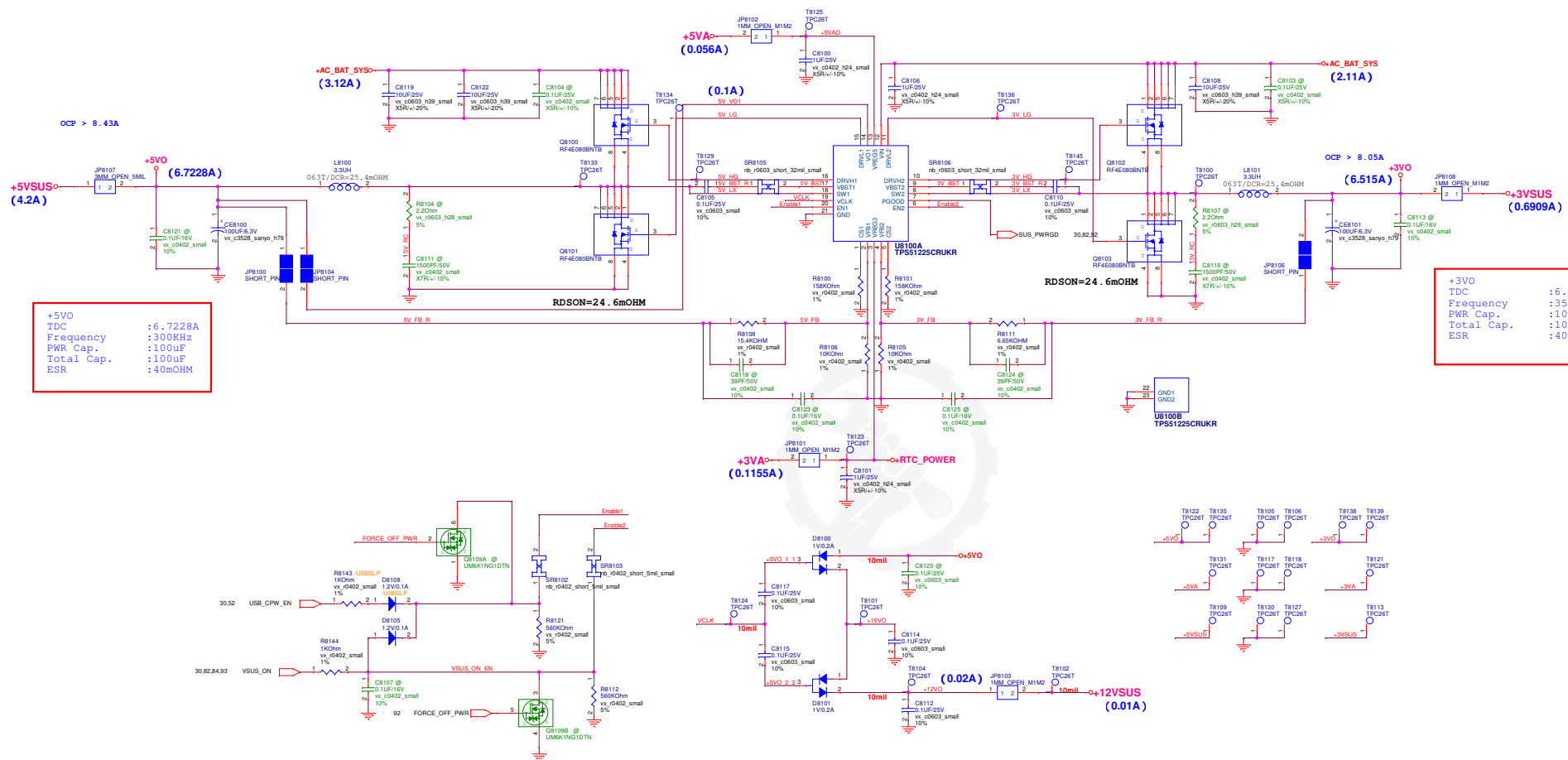
PEGATRON		Title : ****	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Raly Hsieh</i>	
Size A	Project Name GTKUG_25W		Rev 1.0
Date: <u>Tuesday, September 06, 2016</u>		Sheet <u>79</u> of <u>99</u>	

VCORE & VCCGT & VCCSA POWER SUPPLY

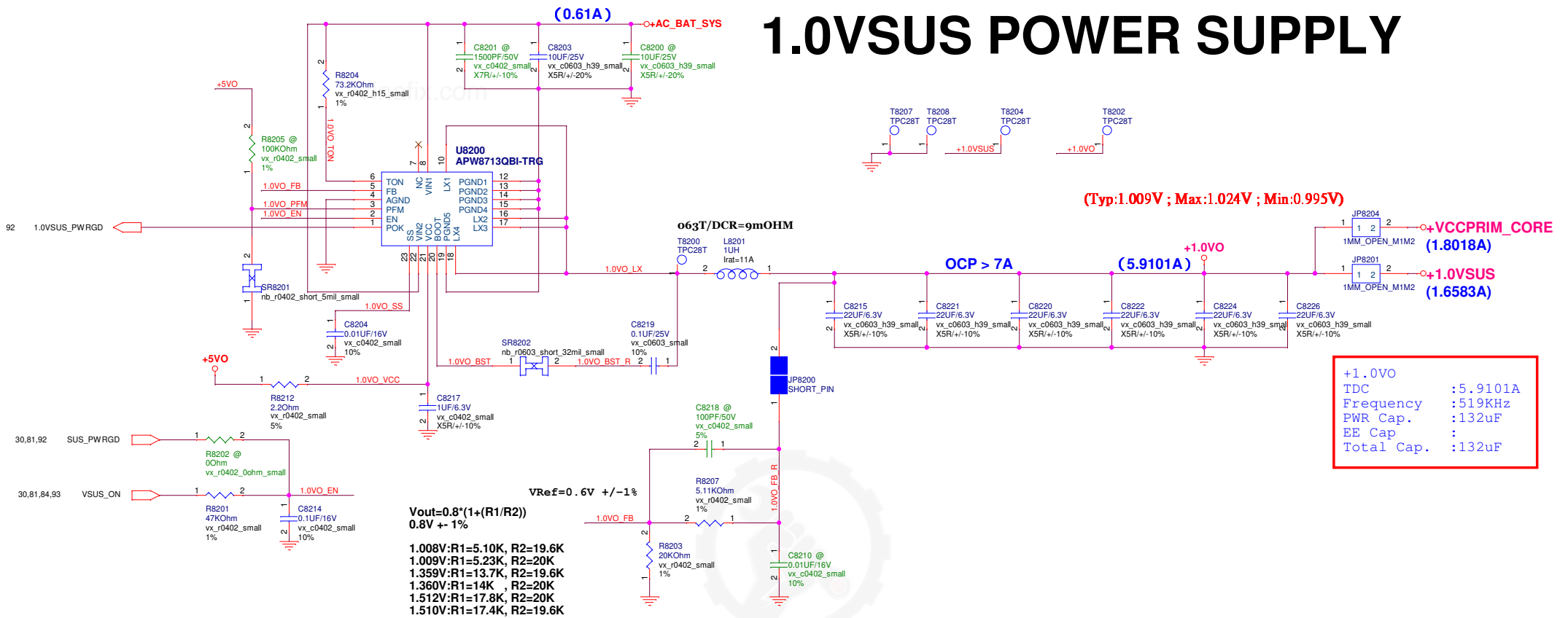


5VO & 3VO POWER SUPPLY

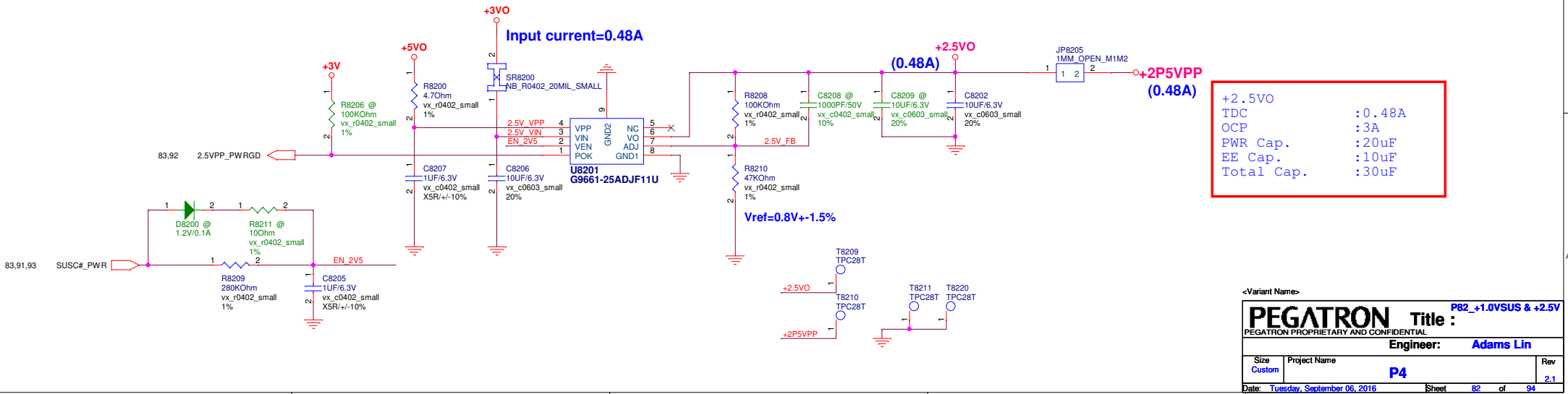
Vinafix.com



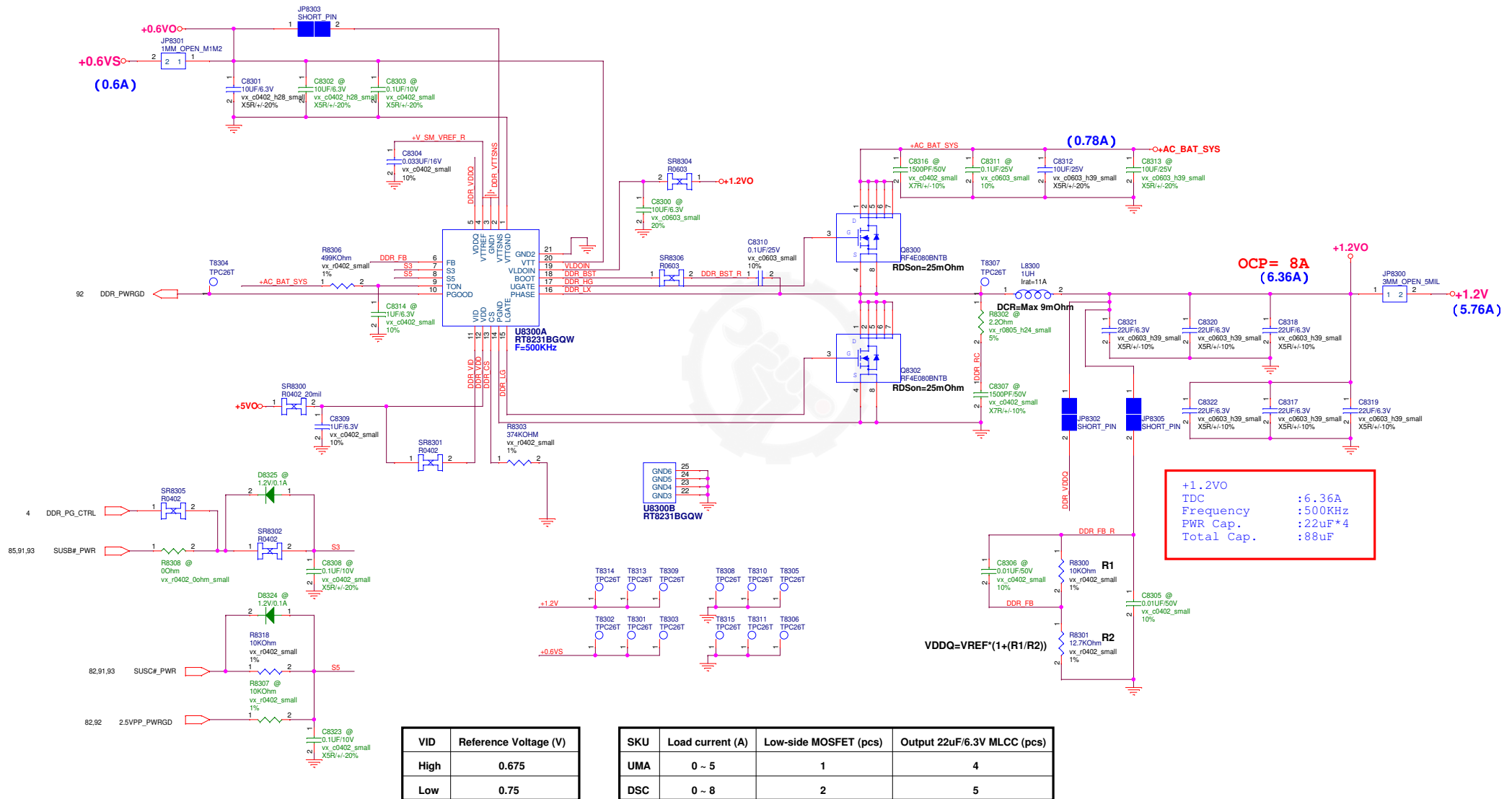
1.0VSUS POWER SUPPLY



2.5V POWER SUPPLY



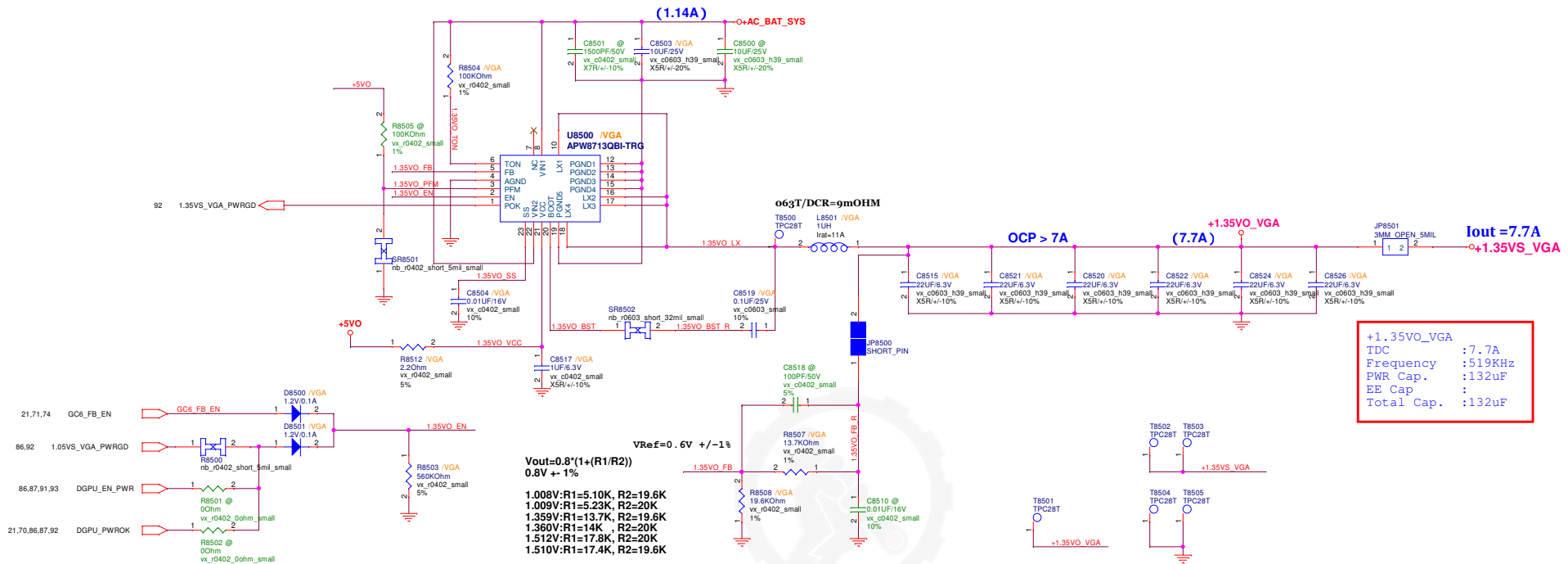
DDR & VTT POWER SUPPLY



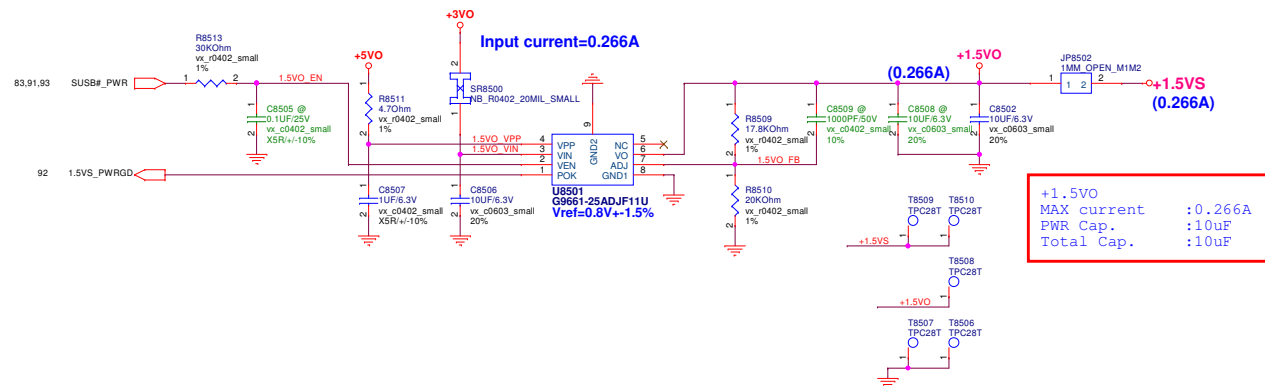
[illegible]

1.35VS_VGA POWER SUPPLY

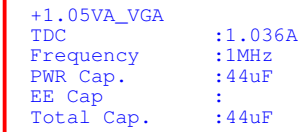
Vinafix.com



1.5VS POWER SUPPLY



<Variant Name>



VGA_CORE POWER SUPPLY

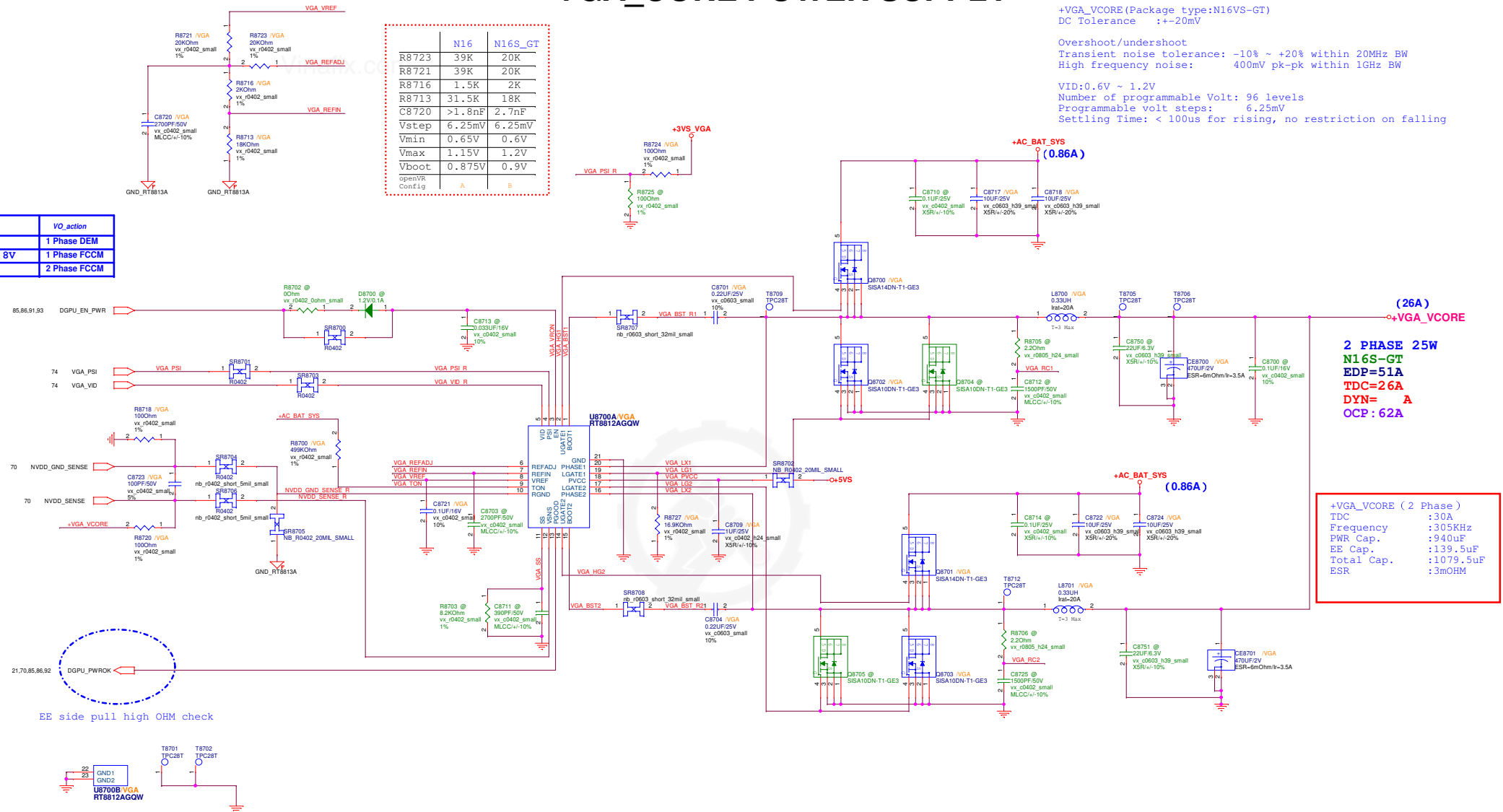
```
+VGA_VCORE(Package type:N16VS-GT)
DC Tolerance      :+-20mV
```

Overshoot/undershoot
Transient noise tolerance: -10% ~ +20% within 20MHz BW
High frequency noise: 400mV pk-pk within 1GHz BW

```
VID:0.6V ~ 1.2V
Number of programmable Volt: 96 levels
Programmable volt steps:      6.25mV
Settling Time: < 100us for rising, no restriction on falling
```

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

	N16	N16S_CT
R8723	39K	20K
R8721	39K	20K
R8716	1.5K	2K
R8713	31.5K	18K
C8720	>1.8nF	2.7nF
Vstep	6.25mV	6.25mV
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.875V	0.9V
openVr		
Config	A	B



<Variant Name>

PEGATRON Title : +VGA_VCORE
PEGATRON PROPRIETARY AND CONFIDENTIAL

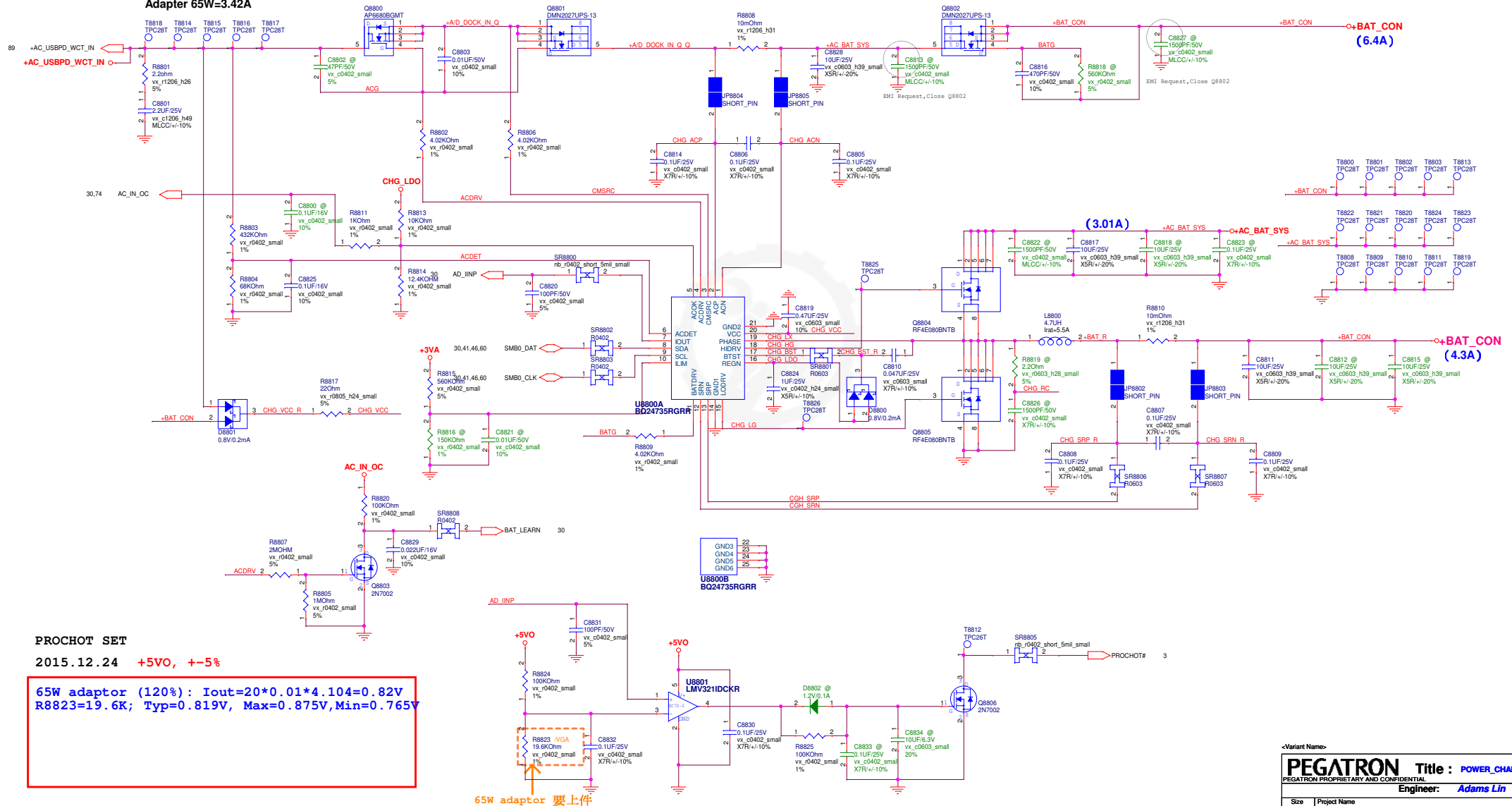
Engineer: *Adams Lin*

Size Custom	Project Name P4	Rev 2.1
Date: Tuesday, September 06, 2016		Sheet 87 of 94

Date: Tuesday, September 06, 2016 Sheet 87 of 94

BATTERY CHARGER

Adapter 65W=3.42A



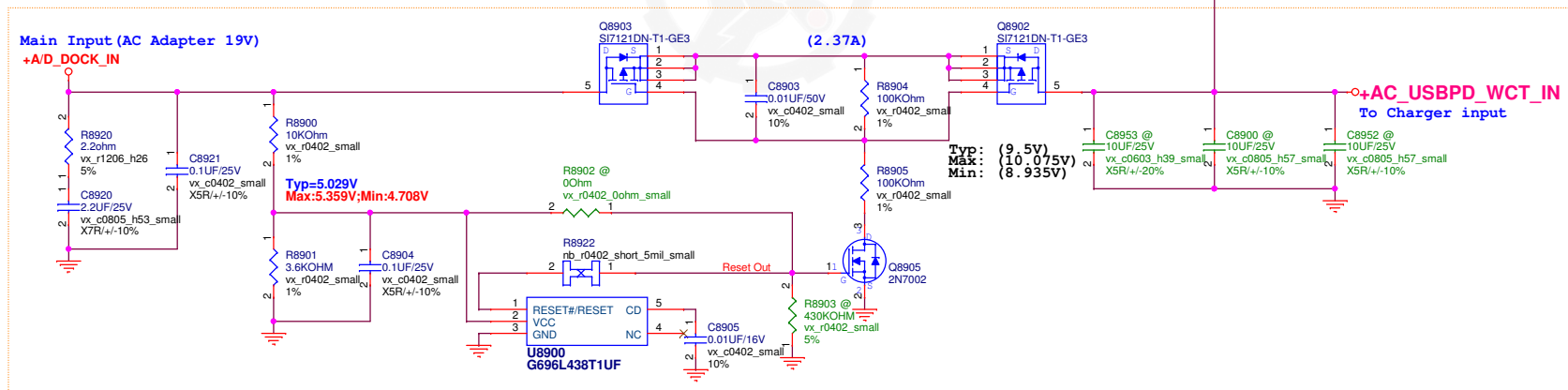
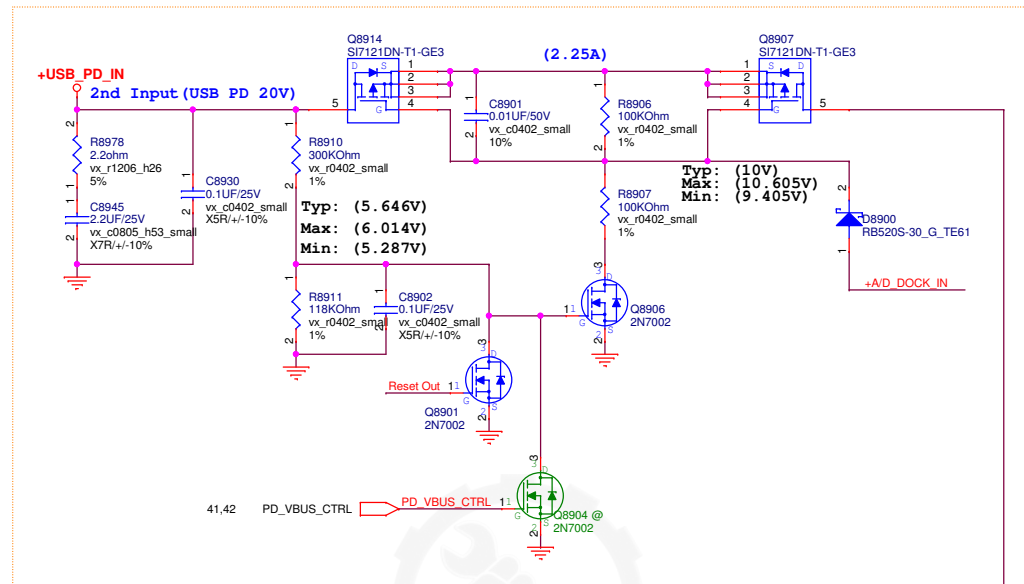
<Variant Name>

PAGATRON Title : POWER_CHARGER
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Adams Lin

Size Custom	Project Name P4	Rev 2.1
Date Tuesday, September 08, 2016	Sheet 86	of 84

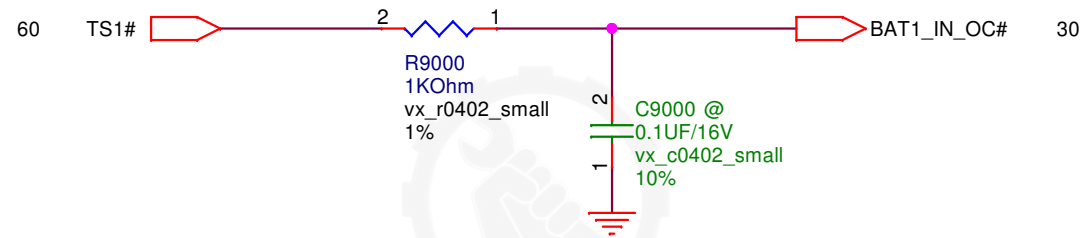
2 Input switch Circuit

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BATTERY IN DETECT



<Variant Name>

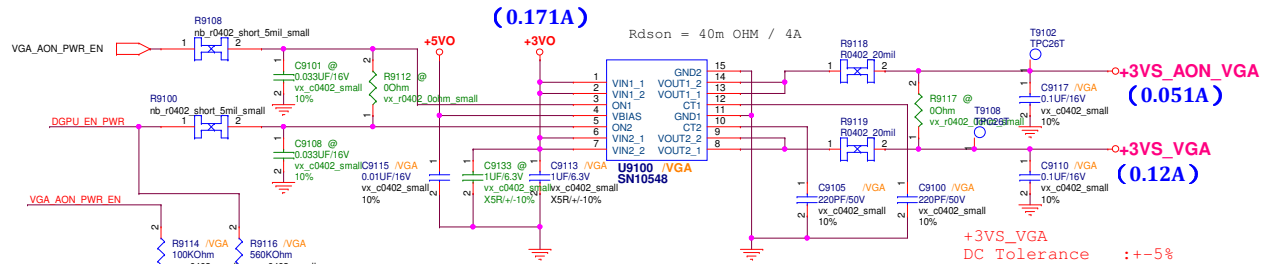
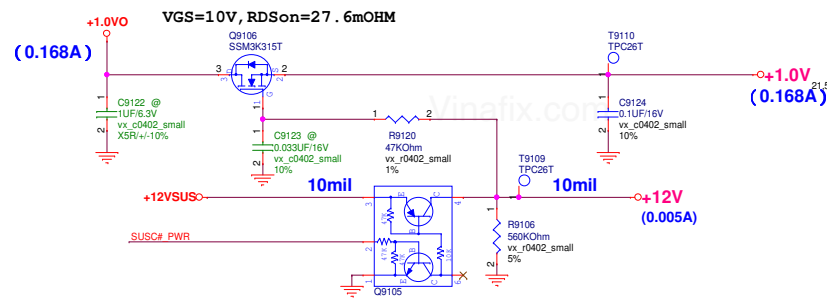
PEGATRON Title : **POWER_DETECT**
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Adams Lin**

Size Custom	Project Name P4	Rev 2.1
----------------	---------------------------	------------

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DSC VGA PWR POWER



```
GC6 Cold boot/Optimus:
3V3_AON & 3V3_MAIN --> NVVDD --> PEX_VDD --> FBVDD/Q
```

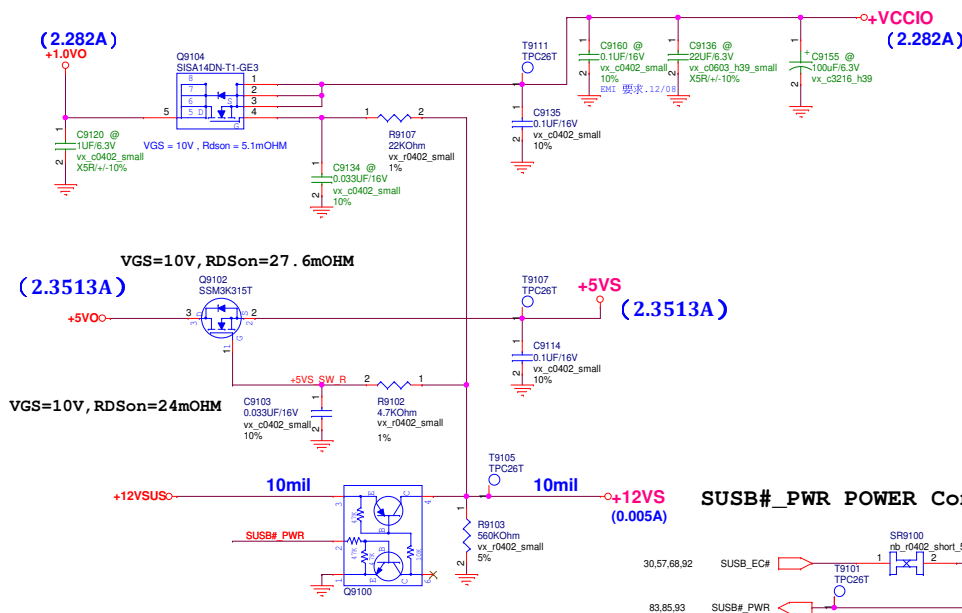
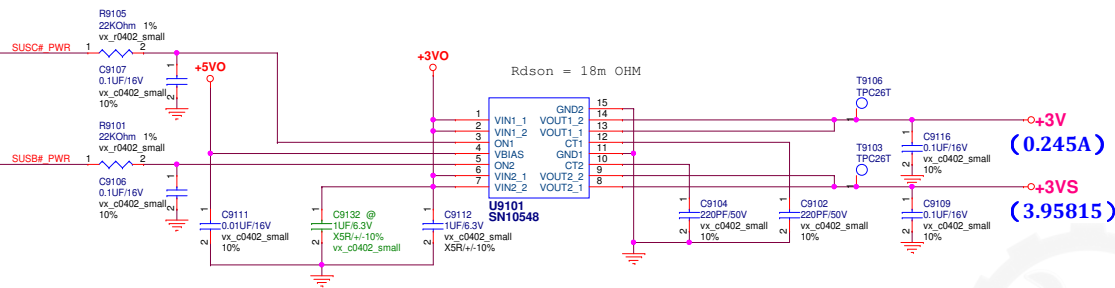
```
GC6 2.0 Exit:
3V3_MAIN --> NVVDD --> PEX_VDD
```

Power up Sequencing

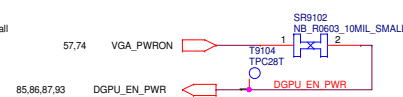
1. The ramp time for any rail must be more 40us and is recommended to be less than 2ms
2. The previous power rail must ramp up to 90% before the next power rail can start ramping up

Power down Sequencing

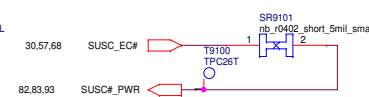
1. There is no specific power down sequence
2. Residual voltage from power down must not violate the power up sequence when back to back GPU power down and power up event take place



DSC_VGA_PWR POWER Control



SUSC#_PWR POWER Control



<Variant Name>

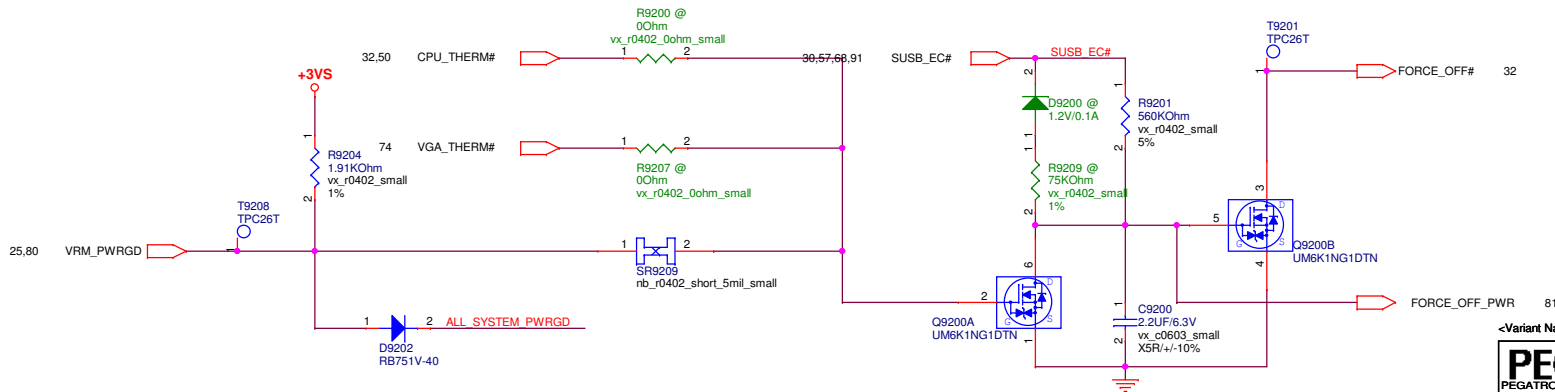
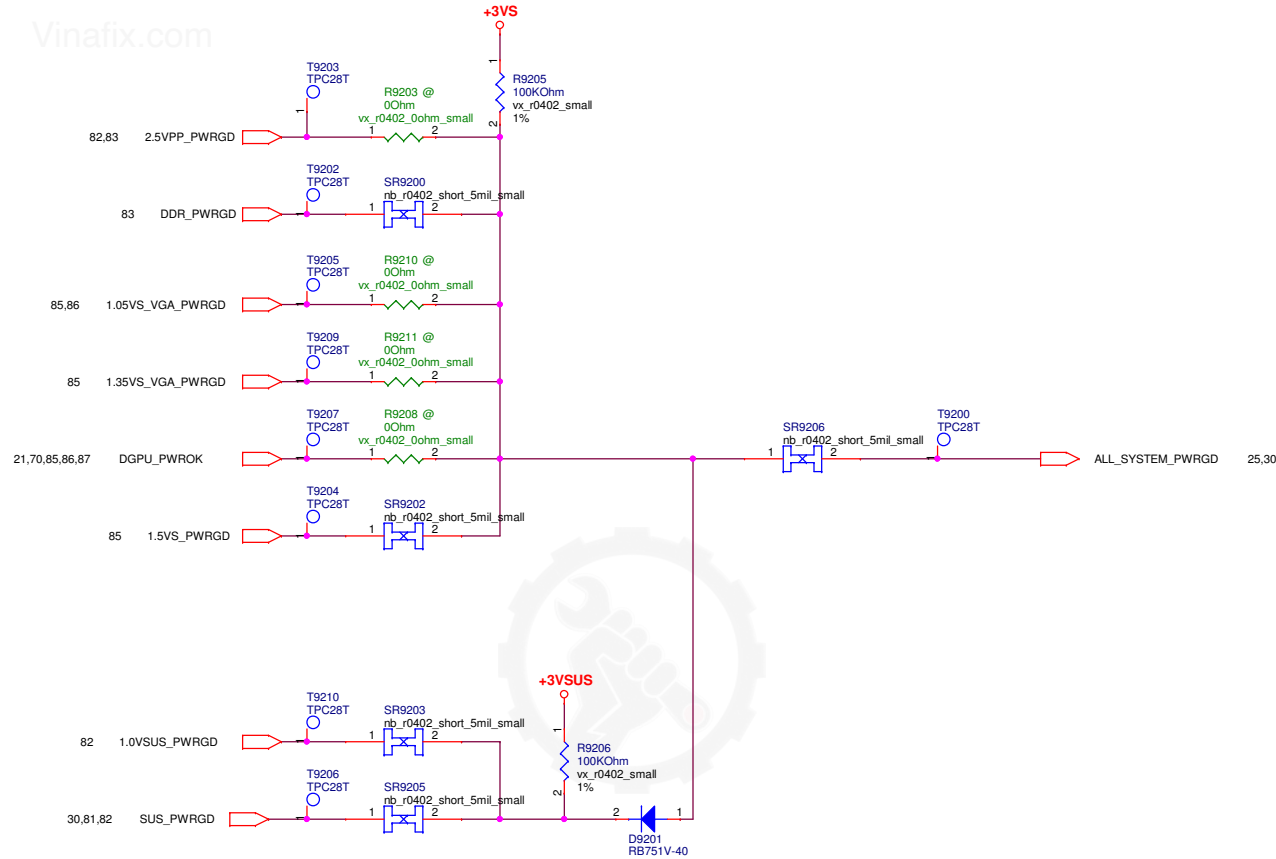
PEGATRON Title : POWER_LOAD SWITCH
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size Custom	Project Name P4	Rev 2.1
Date: Tuesday, September 06, 2016		Sheet 91 of 94

POWER GOOD DETECTOR

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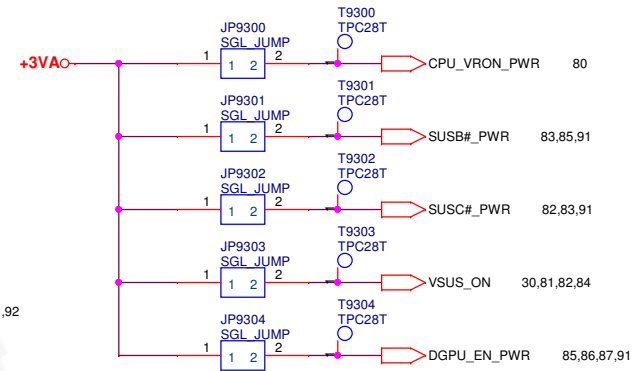


<Variant Name>

PEGATRON		Title : POWER_PROTECT	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		Adams Lin	
Size Custom	Project Name P4	Rev 2.1	
Date:	Tuesday, September 06, 2016	Sheet	92 of 94

+USB_PD_IN	→	+USB_PD_IN	42,89
+A/D_DOCK_IN	→	+A/D_DOCK_IN	60,89
+AC_USBDPD_WCT_IN	→	+AC_USBDPD_WCT_IN	88,89
+AC_BAT_SYS	→	+AC_BAT_SYS	43,45,80,81,82,83,85,87,88
+BAT_CON	→	+BAT_CON	60,88
+RTC_POWER	→	+RTC_POWER	81
+5VA	→	+5VA	31,56,81
+3VA	→	+3VA	24,30,31,36,41,43,53,56,57,67,81,88
+5VO	→	+5VO	26,81,82,83,85,88,91
+3VO	→	+3VO	81,82,84,85,86,91
+2.5VO	→	+2.5VO	82
+1.8VO	→	+1.8VO	84
+1.5VO	→	+1.5VO	85
+1.2VO	→	+1.2VO	83
+1.05VO_VGA	→	+1.05VO_VGA	86
+1.0VO	→	+1.0VO	82,91
+0.6VO	→	+0.6VO	83
+12VSUS	→	+12VSUS	81,91
+5VSUS	→	+5VSUS	41,42,52,56,67,81
+3VSUS	→	+3VSUS	4,24,25,26,28,30,31,33,41,42,51,53,62,67,68,81,92
+1.8VSUS	→	+1.8VSUS	9,21,24,26,84
+1.0VSUS	→	+1.0VSUS	26,82
+12V	→	+12V	91
+2P5VPP	→	+2P5VPP	16,17,57,82
+1.2V	→	+1.2V	4,7,15,16,17,18,57,83
+1.0V	→	+1.0V	7,57,91
+12VS	→	+12VS	28,31,57,62,91
+5VS	→	+5VS	31,36,45,46,48,50,51,56,57,67,80,87,91
+3VS	→	+3VS	3,4,17,20,21,22,23,24,28,30,31,32,36,37,45,46,47,48,50,51,53,57,61,62,67,91,92
+1.5VS	→	+1.5VS	36,57,85
+1.05VS_VGA	→	+1.05VS_VGA	57,70,71,72,86
+0.6VS	→	+0.6VS	15,17,57,83
+VCORE	→	+VCORE	5,57,80
+VCCGT	→	+VCCGT	6,57,80
+VCCSA	→	+VCCSA	7,57,80
+VCCIO	→	+VCCIO	3,7,57,91
+VCCPRIM_CORE	→	+VCCPRIM_CORE	26,82
+VGA_VCORE	→	+VGA_VCORE	57,75,87

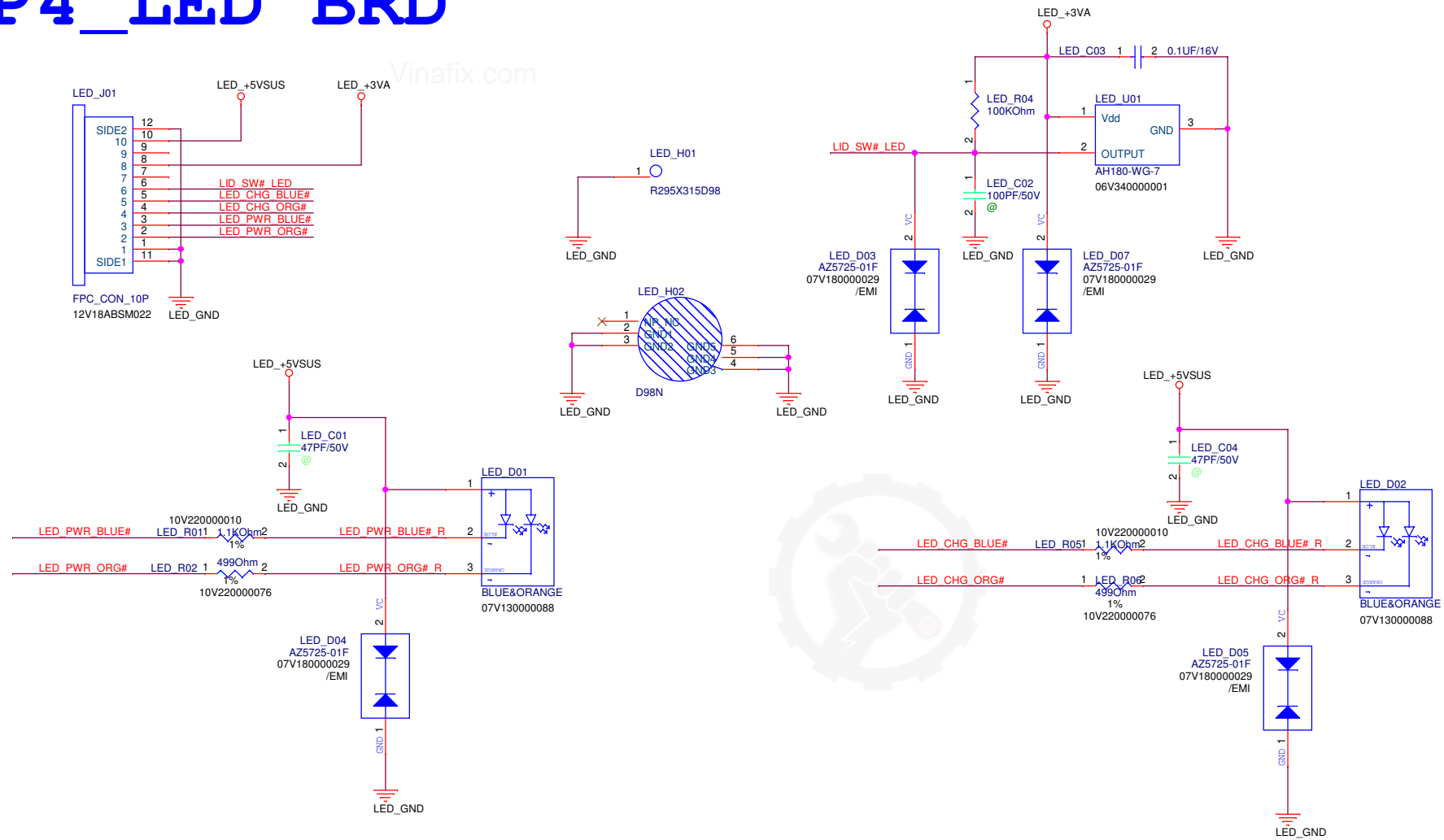
FOR POWER TEST



PEGATRON		Title : POWER_SIGNAL	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-POWER		Engineer: Adams Lin	
Size B	Project Name P4	Rev 2.1	
Date: Tuesday, September 06, 2016		Sheet 93 of 94	

P4_LED BRD

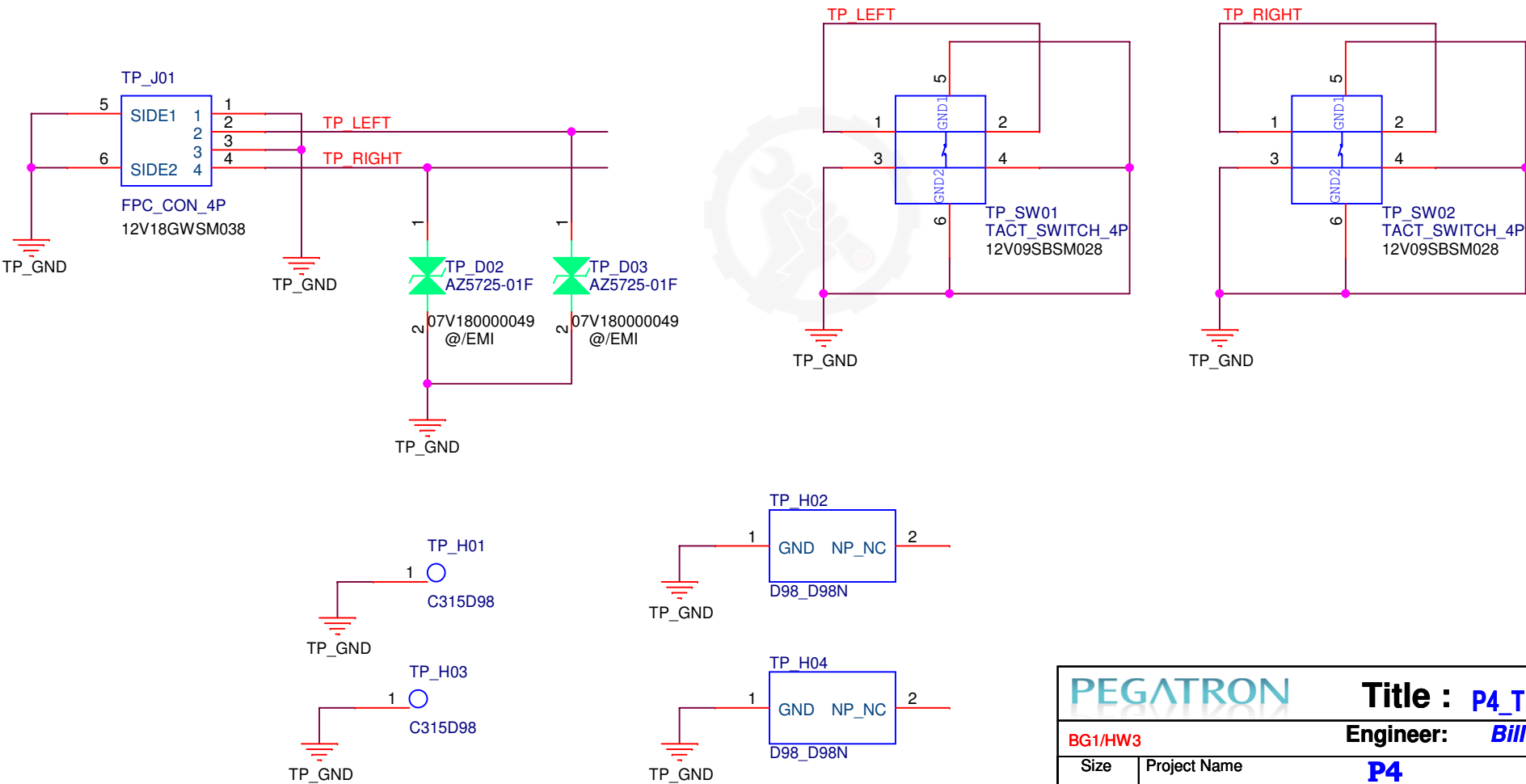
Vinafix.com



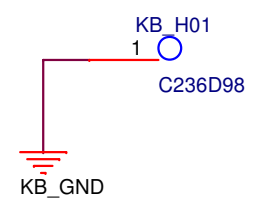
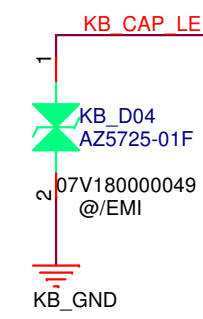
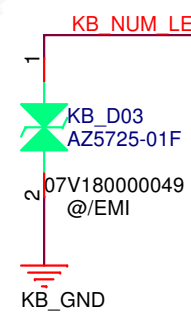
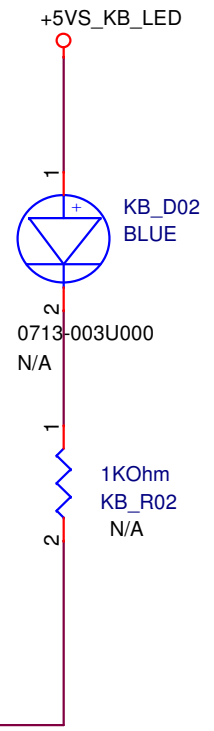
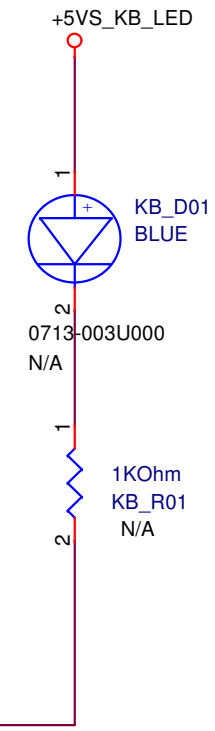
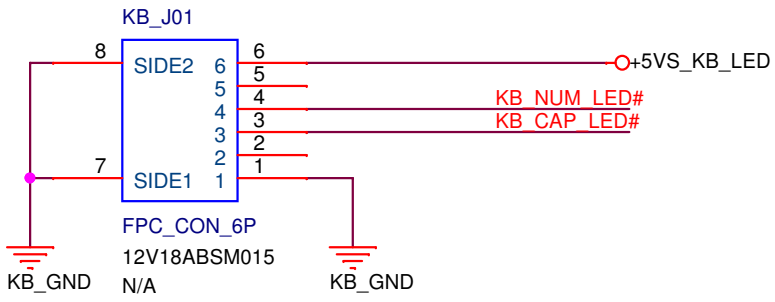
P4_TP-button BRD

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TP_BRD to TP_Model



PEGATRON		Title : P4_TP-button BRD	
BG1/HW3		Engineer: Bill Yang	
Size	Project Name		Rev
Custom	P4		1.0
Date: Tuesday, September 06, 2016		Sheet	105 of 110



PEGATRON		Title : P4_KB_LED	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Bill Yang	
Size	Project Name		Rev
Custom	P4		1.1
Date: Tuesday, September 06, 2016		Sheet 106 of 108	